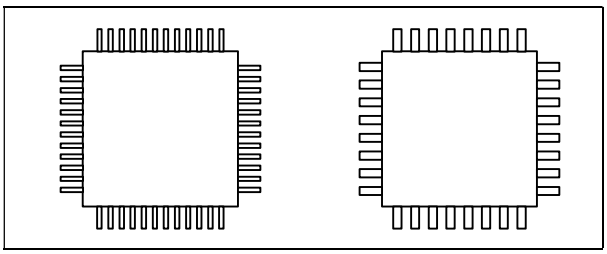
FP5600

192-MHz 32-bit MCUs, Cortex®-M0+ Core, 91.2 DMIPS,
12-bit ADC (equipped with 2 S/H circuits, 20 data registers, and 4 digital comparators)
192-MHz PWM (three-phase motor PWM output × 2 channel)

32-Bit ARM® Cortex®-M0+ MCU

Features

- **ARM® Cortex®-M0+ Core**
  - Capable of 91.2 DMIPS in operation at 96 MHz
- **Power management**
  - Wide voltage range operation: 2.7 to 5.5 V
  - Minimum power consumption during sleep mode is less than 3 μA
  - Built-in BOD and POR circuit
- **Memories:**
  - 64KB Flash memory
  - 16KB RAM
  - Flash accelerator, which provides faster code efficiency and can emulate EEPROM to store data
- **DMA**
  - 4-channel DMA
- **Clock functions**
  - High-precision built-in internal clock, PLL can generate up to 192 MHz PWM clock
  - CPU main frequency up to 96 MHz
  - Supports external high-speed crystal oscillators
- **Motor Control Accelerator**
  - Supports up to dual motor FOC (Field Oriented Control) sine wave control
  - PFC (Power Factor Correction)
  - Built-in CORDIC math hardware accelerator to speed up motor control operations, including trigonometric functions and dividers
  - Built-in square wave decoder, can support motor position optical encoder
- **Up to 6 communications channels**
  - UART (3 channels)
  - SPI (1 channel)
  - I^2C (1 channel)
- **Timers**
  - 16-bit 6-channel timer for motor PWM output (2 channels/1 channel)
  - 16-bit 1-channel timer for input capture and basic PWM output (3 channels)
  - Watchdog timer
  - RTC
  - General timer (2 channels)
- **12-bit ADC (16 channels/11 channels)**
  - 0.8 μs conversion time, with two sample-and-hold circuits
  - Supports accurate simultaneous sampling of dual currents
  - Multiple trigger sources
- **Motor overcurrent protection**
  - 4 PGAs (Programmable Gain Amplifier) , which can realize current signal amplification
  - 4 comparators, which can realize current protection and motor back EMF detection functions
- **Built-in two 6-bit DACs** for comparator use and a 10-bit DAC for user debugging
- **Operating temperature range:** -40 ~ 105 °C
- **High reliability**
  - ESD 4 kV
  - EFT 4 kV
- **Packages**
  - 48-pin LQFP
  - 32-pin LQFP



LQFP48 7x7 mm　　LQFP32 7x7 mm

Overview

The FP5600 microcontroller integrates ARM® Cortex®-M0+ 32-bit core operating up to 96 MHz, on-chip memory including 64KB Flash, 16KB SRAM. Flash accelerator provides faster code efficiency and can emulate EEPROM to store data. The clock function of FP5600 includes high-precision built-in internal clock, and PLL can generate up to 192 MHz PWM clock. The FP5600 supports external high-speed crystal oscillators. The FP5600 offers communication interfaces (three UART, one SPI and one I^2C).

The FP5600 has wide voltage range operation (2.7 to 5.5 V), temperature range -40 ~ 105 °C, and the lowest power consumption is less than 3 μA in sleep mode. FP5600 has built-in BOD and POR circuits. As for the high reliability part, the FP5600 has ESD 4 kV and EFT 4 kV.

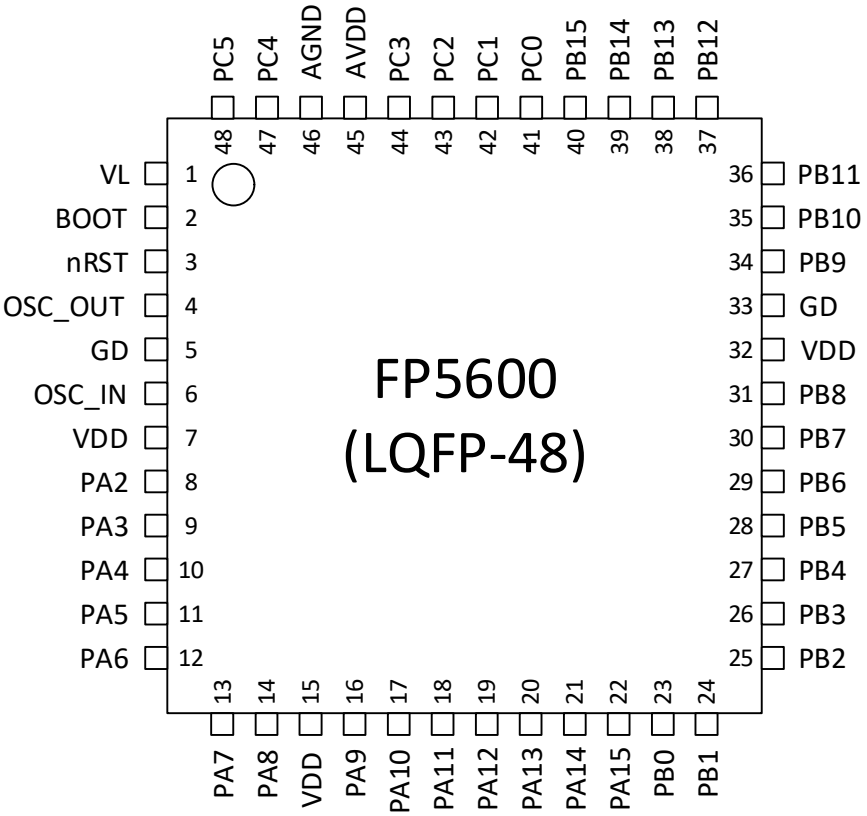
The FP5600 microcontroller built in CORDIC math hardware accelerator to increase the efficiency of motor control operations, including trigonometric functions and dividers. For motor angle detection, the FP5600 has built-in square wave decoder, which can support motor position optical encoder. The FP5600 supports up to two motor FOC (Field Oriented Control) sine wave control and PFC (Power Factor Correction).

The FP5600 has up to 16 channels 12-bit ADC, with 0.8 μs conversion time, two sample-and-hold circuits, which support accurate simultaneous sampling of dual currents and multiple trigger sources. The FP5600 comes with 4 PGAs (Programmable Gain Amplifier), and 4 comparators, which can realize current amplification, protection and motor back EMF detection functions. The FP5600 built in two 6-bit DACs for comparator use and a 10-bit DAC for user debugging.

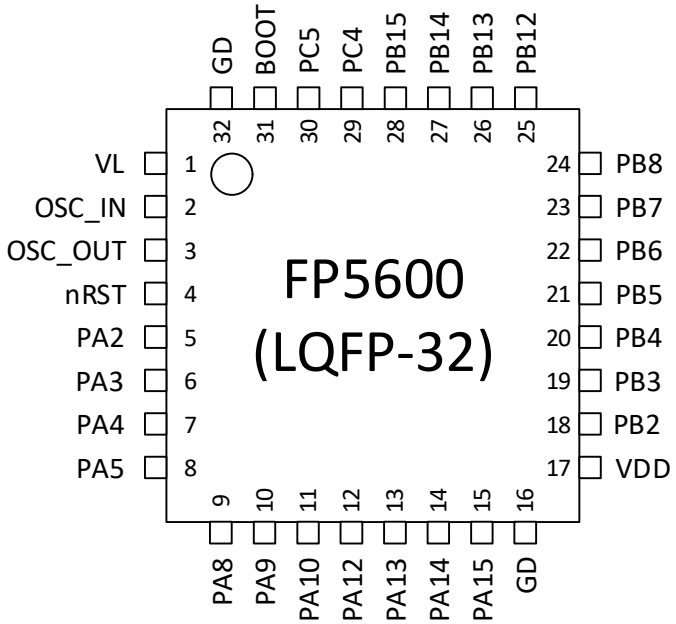
The FP5600 is offered in 48 pin and 32 pin LQFP packages.

Pin Assignments

LQFP Package: LQFP-48



LQFP Package: LQFP-32



Contents

1. Pin Functions

48 Package

48 Pin	PIN Name	IO Wake Up	ANA_CH	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
1	VL										
2	BOOT										
3	nRST										
4	OSC_OUT		OSC_OUT								
5	GD										
6	PA1-OSC_IN		OSC_IN								
7	VDD										
8	PA2	V	AIO_14	ACMP1_O	MTPWM0_BRAKE_2	MTPWM0_BRAKE_0	ETIMER1_CH	ACOMP0_O	UART2_TX		
9	PA3		AIO_13	SPI0_CS		IDX0	ETIMER2_CH		UART0_RX		
10	PA4		AIO_12	SW_CLK							
11	PA5		AIO_11	SW_DIO							
12	PA6		AIO_10	SPI0_CLK		QEI0_A			UART0_TX	SPI0_MOSI	I2C0_SDA
13	PA7		AIO_9	SPI0_MISO	MTPWM1_BRAKE_1				UART1_RX		I2C0_SCL
14	PA8		AIO_8	SPI0_MOSI	UART0_RX	IDX1	QEI0_B		UART1_TX		I2C0_SDA
15	VDD										
16	PA9	V			MTPWM0_BRAKE_1	SPI0_CS	ETIMER0_CH				
17	PA10			ETIMER0_CH		QEI1_A				SPI0_CLK	
18	PA11			ACMP3_O	MTPWM0_BRAKE_0	QEI1_B			UART2_TX	SPI0_MOSI	I2C0_SDA
19	PA12	V		MTPWM1_2B	MTPWM0_BRAKE_0	IDX1			UART2_RX	SPI0_MISO	I2C0_SCL
20	PA13			MTPWM1_1B	ETIMER0_CH	IDX0	ETIMER2_CH			SPI0_MOSI	
21	PA14			MTPWM1_0B	ETIMER1_CH			ACOMP1_O		SPI0_CS	
22	PA15			MTPWM1_2A			ETIMER2_CH	ACOMP2_O		SPI0_CS	
23	PB0			MTPWM1_1A						SPI0_MISO	
24	PB1	V		MTPWM1_0A						SPI0_CLK	
25	PB2			MTPWM0_2B		MTPWM0_1B	MTPWM0_0B	ACOMP3_O		SPI0_CLK	
26	PB3			MTPWM0_1B	I2C0_SCL	MTPWM0_2A	MTPWM0_1B	ACOMP1_O	UART0_TX	SPI0_CS	
27	PB4			MTPWM0_0B	I2C0_SDA	MTPWM0_2B	MTPWM0_2B	ACOMP2_O	UART0_RX		
28	PB5			MTPWM0_2A	MTPWM0_BRAKE_1		QEI0_A	ACOMP3_O	UART1_TX		
29	PB6			MTPWM0_1A	MTPWM0_BRAKE_2		QEI0_B	ACOMP0_O	UART1_RX		
30	PB7			MTPWM0_0A	SW_DIO		IDX0	ETIMER0_CH	UART2_RX	SPI0_MISO	SPI0_MOSI
31	PB8			MTPWM0_BRAKE_0	SW_CLK			ETIMER1_CH		SPI0_CLK	I2C0_SCL
32	VDD										
33	GD										
34	PB9			ACMP0_O	MTPWM1_BRAKE_2		ETIMER0_CH			SPI0_CLK	
35	PB10			ETIMER1_CH	CLOCK_O			ACOMP1_O		SPI0_MOSI	
36	PB11			ACMP2_O		IDX0	ETIMER2_CH			SPI0_MISO	
37	PB12		AIO_7	UART0_RX	MTPWM0_0A	MTPWM0_0A		ACOMP3_O		SPI0_CS	
38	PB13		AIO_6	UART0_TX	MTPWM0_0B	MTPWM0_1A				SPI0_CLK	
39	PB14		AIO_5	I2C0_SCL	MTPWM0_1A	MTPWM0_2A	ETIMER0_CH			SPI0_MISO	
40	PB15		AIO_4	I2C0_SDA	MTPWM0_1B	MTPWM0_0B	ETIMER1_CH			SPI0_MOSI	
41	PC0		AIO_3								
42	PC1		AIO_2								
43	PC2		AIO_1								
44	PC3		AIO_0								
45	AVDD										
46	AGND										
47	PC4		AIO_15		MTPWM0_2A	QEI0_A	ETIMER0_CH	ACOMP0_O	MTPWM0_1B	UART1_TX	I2C0_SCL
48	PC5		AIO_16 (VREF)		MTPWM0_2B	QEI0_B	ETIMER1_CH	ACOMP2_O	MTPWM0_2B	UART1_RX	I2C0_SDA

32 Package

32 Pin	PIN Name	IO Wake Up	ANA_CH	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
1	VL										
2	OSC_IN		OSC_IN								
3	OSC_OUT		OSC_OUT								
4	nRST										
5	PA2	V	AIO_14	ACMP1_O	MTPWM0_BRAKE_2	MTPWM0_BRAKE_0	ETIMER1_CH	ACOMP0_O	UART2_TX		
6	PA3		AIO_13	SPI0_CS		IDX0	ETIMER2_CH		UART0_RX		
7	PA4		AIO_12	SW_CLK							
8	PA5		AIO_11	SW_DIO							
9	PA8		AIO_8	SPI0_MOSI	UART0_RX	IDX1	QEI0_B		UART1_TX		I2C0_SDA
10	PA9	V			MTPWM0_BRAKE_1	SPI0_CS	ETIMER0_CH				
11	PA10			ETIMER0_CH		QEI1_A				SPI0_CLK	
12	PA12	V		MTPWM1_2B	MTPWM0_BRAKE_0	IDX1			UART2_RX	SPI0_MISO	I2C0_SCL
13	PA13			MTPWM1_1B	ETIMER0_CH	IDX0	ETIMER2_CH			SPI0_MOSI	
14	PA14			MTPWM1_0B	ETIMER1_CH			ACOMP1_O		SPI0_CS	
15	PA15			MTPWM1_2A			ETIMER2_CH	ACOMP2_O		SPI0_CS	
16	GD										
17	VDD										
18	PB2			MTPWM0_2B		MTPWM0_1B	MTPWM0_0B	ACOMP3_O		SPI0_CLK	
19	PB3			MTPWM0_1B	I2C0_SCL	MTPWM0_2A	MTPWM0_1B	ACOMP1_O	UART0_TX	SPI0_CS	
20	PB4			MTPWM0_0B	I2C0_SDA	MTPWM0_2B	MTPWM0_2B	ACOMP2_O	UART0_RX		
21	PB5			MTPWM0_2A	MTPWM0_BRAKE_1		QEI0_A	ACOMP3_O	UART1_TX		
22	PB6			MTPWM0_1A	MTPWM0_BRAKE_2		QEI0_B	ACOMP0_O	UART1_RX		
23	PB7			MTPWM0_0A	SW_DIO		IDX0	ETIMER0_CH	UART2_RX	SPI0_MISO	SPI0_MOSI
24	PB8			MTPWM0_BRAKE_0	SW_CLK			ETIMER1_CH		SPI0_CLK	I2C0_SCL
25	PB12		AIO_7	UART0_RX	MTPWM0_0A	MTPWM0_0A		ACOMP3_O		SPI0_CS	
26	PB13		AIO_6	UART0_TX	MTPWM0_0B	MTPWM0_1A				SPI0_CLK	
27	PB14		AIO_5	I2C0_SCL	MTPWM0_1A	MTPWM0_2A	ETIMER0_CH			SPI0_MISO	
28	PB15		AIO_4	I2C0_SDA	MTPWM0_1B	MTPWM0_0B	ETIMER1_CH			SPI0_MOSI	
29	PC4		AIO_15		MTPWM0_2A	QEI0_A	ETIMER0_CH	ACOMP0_O	MTPWM0_1B	UART1_TX	I2C0_SCL
30	PC5		AIO_16 (VREF)		MTPWM0_2B	QEI0_B	ETIMER1_CH	ACOMP2_O	MTPWM0_2B	UART1_RX	I2C0_SDA
31	BOOT										
32	GD										

2. Application Circuit

As shown in Figure 2-1, the FP5600 supports up to dual motor FOC (Field Oriented Control) sine wave control. There are 4 PGAs (Programmable Gain Amplifier) for realizing current signal amplification, and 4 analog comparators for realizing current protection and motor back EMF detection functions.

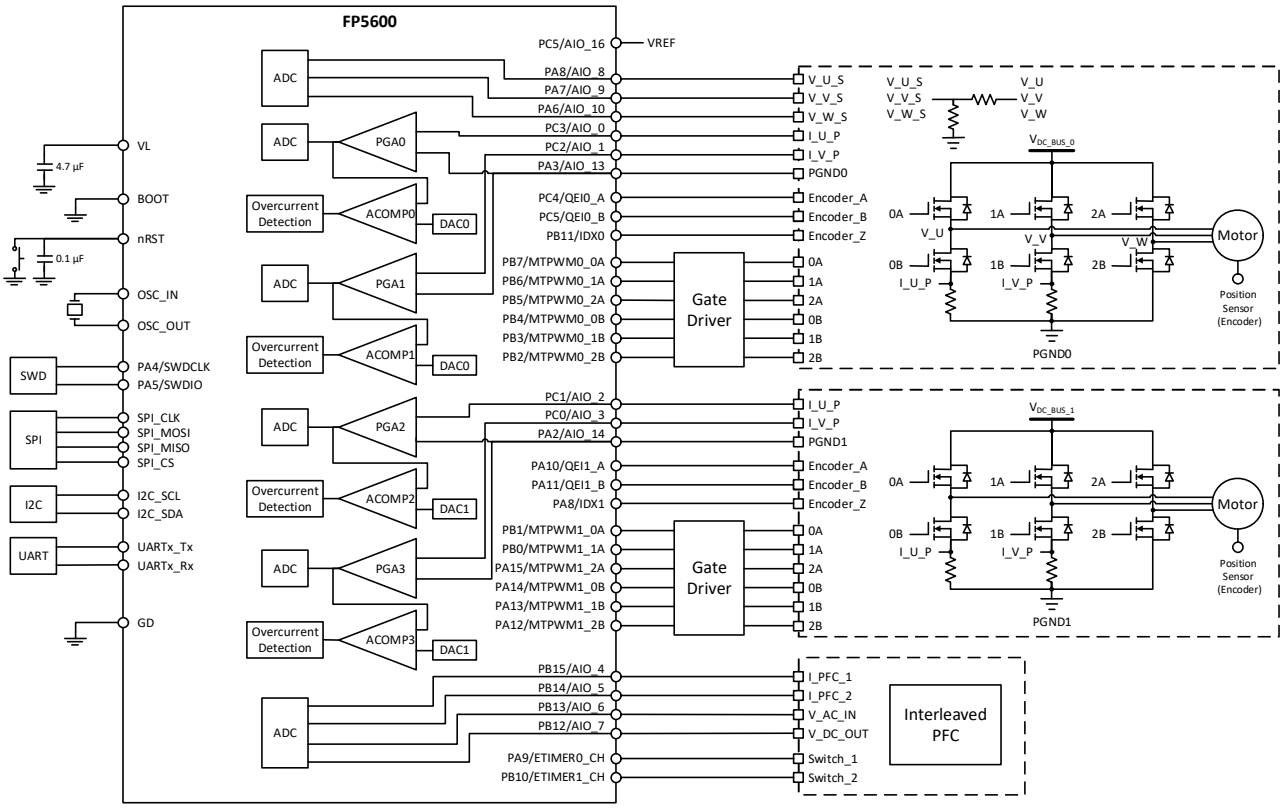
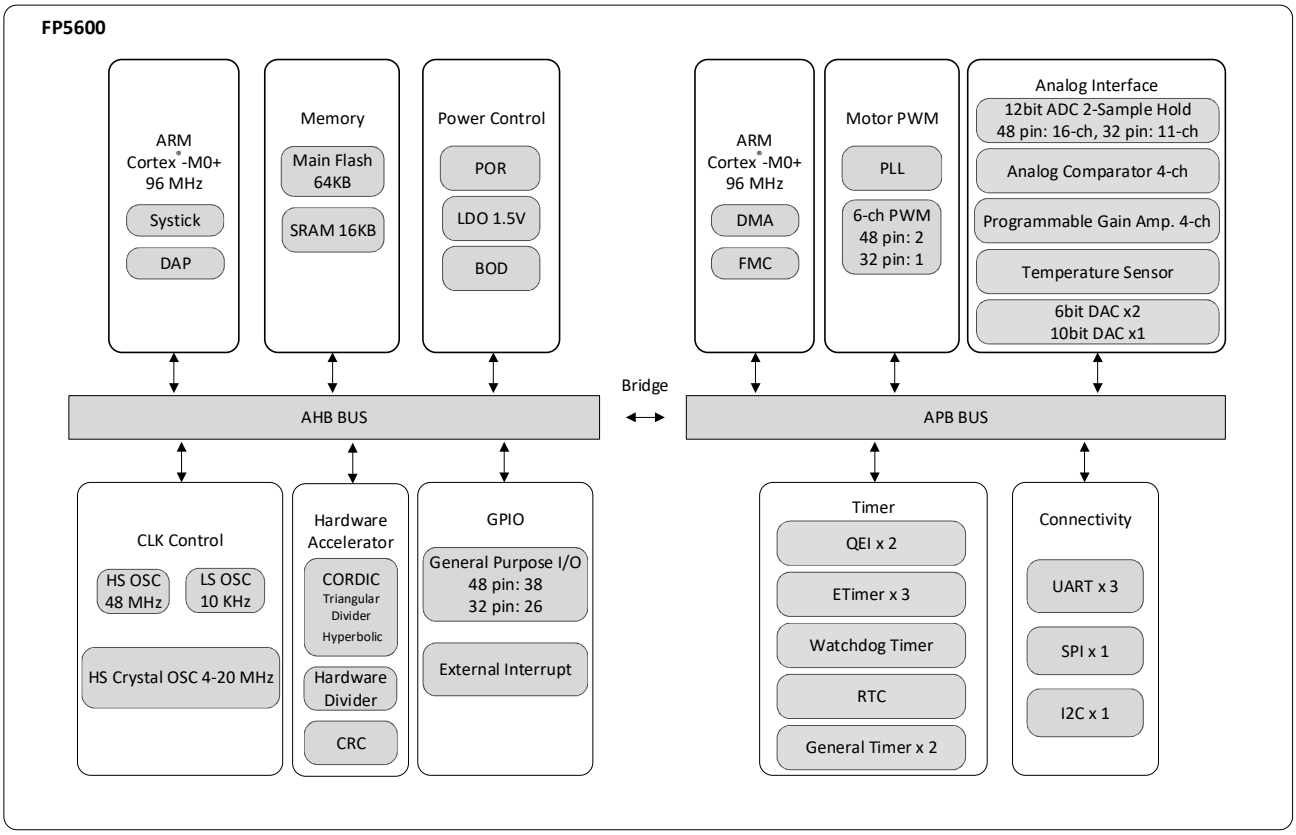


Figure 2-1 FP5600 application circuit

3. Function Block



4. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Processor						
RAM				16		Kbyte
FLASH				64		Kbyte
Processor speed			0.01	96	96	MHz
General Supply						
Operation Voltage	V_{DD}		2.8	5 or 3.3	5.5	V
LDO Output Voltage	V_L	It is recommended a 0.1uF bypass capacitor		1.65		V
Supply Current (Normal)	I_{DD}			31.78	36.41	mA
Supply Current (Sleep Mode)	I_{DD}			3.938	20	μA
Operation Temperature	T_{OPER}		-40		105	℃
LDO Output Voltage(PLL)	V_{PLL}			1.5		V
Power On/Down Reset						
Power On VDD Threshold(Rising Voltage)	V_{POR}			1.8		V
Power Down VDD Threshold	V_{PDR}			1.6		V
Hysteresis	V_{POR_HYS}			200		mV
POR Reset Delay Time	t_{POR}	DIP debounce,		1.6		ms
Operating Current	I_{POR}	Alive anytime		1		μA
Brown-out Detector						
Brown-Out Level	V_{BO}		2.3	8 level unit(volt) 0: 2.3 1: 2.6 2: 2.9 3: 3.2 4: 3.5	4.4	V

				5: 3.8 6: 4.1 7: 4.4		
Hysteresis	V_{BO_HYS}			100		mV
Deglitch Time	$t_{BO\_DEGLITH}$			100		μs
Operating Current	I_{BO}			75		μA
High Speed Internal RC Oscillator (HIRC)						
Operation Voltage	V_L			1.5		V
Operation Current	I_{HIRC}			300		μA
Center Frequency	F_{HIRC}			48		MHz
Absolute Frequency Accuracy		@ 25°C VDD 5V,3.3V	-1		1	%
Calibrated Internal Oscillator Frequency		@ -40~105°C	-2		+2	%
Low Speed Internal RC Oscillator (LIRC)						
Operation Voltage	V_{DD}	Alive anytime		V_{DD}		V
Center Frequency	F_{LIRC}			10		kHz
Calibrated Internal Oscillator Frequency		@ -40~105°C VDD=2.3~5.5V	-15%		+15	%
Operating Current	I_{LIRC}			2		μA
High Speed External Crystal (HXT)						
Clock Frequency	F_{HXT}		4		20	MHz
Operation Voltage	V_{DD}	@ -40~125°C	1.8	5	5.5	V
Operating Current	I_{HXT}	@16MHz 5.5V		670		μA
Load Capacitance	C_{HXT}	*1			100	fF
Phase Locked Loop (PLL) and Chip Clock Management						

PLL / PDU Operating Frequency	CKOUT		144		192	MHz
Operation Voltage	V_{PLL}			V_{PLL}		V
Input Clock MCLK Range	CLK_EXT		6		48	MHz
PLL Lock Time	t_{PLL_LOCK}			100	1000	μs
OSC (internal oscillator)	f_{HIRC}		46.56	48	49.44	MHz
CLK_EXT jitter			-200		+200	ps
Operating Current	I_{PLL}			3		mA
ADC Specification						
ADC Bit				12		Bit
Operation Voltage	V_{DD}		2.8		5.5	V
Sample and Hold				2		
ENOB	ENOB	at V_{ref}=4.096V, V_{DD} *1	10	10.5	11	
ADC Full Range Reference Voltage	V_{ADC}	Only confirm trim V_{ref}=4.096V @ V_{DD}=5V *1		V_{ref}=V_{DD} V_{ref}=External V_{ref}=4.096V		V
Date conversion rate	f_{DATA_RATE}	ADC_CLK =T = 24 MHz ADCCTL1. COREDIV[5:0]=03h *1		1		MHz
Acquisition time	t_{ACQ}	ADC_CLK =T = 24 MHz ADCCTL1. COREDIV[5:0]=03h *1		200		ns
Conversion time	t_{CONV}	ADC_CLK =T = 24 MHz ADCCTL1. COREDIV[5:0]=03h *1		800		ns
Differential Linearity	DNL	at V_{DD}=5V, V_{ref}=V_{DD} *1	-1		+1	LSB
Integral Non-Linearity	INL	at V_{DD}=5V, V_{ref}=V_{DD} *1	-2		+2	LSB
Offset Error		at V_{DD}=5V, V_{ref}=4.096V, V_{in}=5%V_{ref}		±5	±6.5	LSB
Offset Drift		at V_{DD}=5V, V_{ref}=4.096V, -40 ~ 105 °C *1		180		μV/℃
Gain Error		at V_{DD}=5V, V_{ref}=4.096V, V_{in}=5%~95%V_{ref}		±5	±6.5	LSB
Gain Drift		at V_{DD}=5V, V_{ref}=4.096V, -40 ~ 105 °C *1		-140		μV/℃
Absolute Error		at V_{DD}=5V, V_{ref}=4.096V		±7		LSB
Linear Range of ADC		at V_{DD}=V_{ref}=4.096V	5		95	%

SFDR	SFDR	at input frequency<1K Hz *1	67	75		dB
SINAD	SINAD	at input frequency<1K Hz *1	62	65	68	dB
SNR	SNR	at input frequency<1K Hz *1	63	66	69	dB
THD	THD	at input frequency<1K Hz *1	-67	-74		dB
Operating Current	I_{ADC}			9.07		mA
Reliability						
Latch up	I_{LATCH_UP}			200		mA
ESD(HBM)	ESD		4			kV
EFT(IO Transmission)	EFT		2			kV
EFT(Power)	EFT		4			kV
PGA						
Input Offset	V_{IN_OFFSET}	*1		±2		mV
Input Offset Drift Avg				2	3.5	μV/℃
Output Swing(V)	V_{OUT_SWING}		0.1		V_{DD}-0.1	V
Input Swing(V)	V_{IN_SWING}	@V_{DD} = 3V, Input +-250mV,V_{com}=1.25V			V_{DD}-1.5	
Input com voltage	V_{IN_COM}		0		V_{DD}-1.5	V
Gain Accuracy				±2		%
Close Loop Gain				1,2,4,8,16,32		V/V
DC gain		*1	60	80		dB
Bandwidth	BW	*1		5		MHz
Phase Margin	PM	*1		50		degree
PSRR	PSRR	*1		70		dB
CMRR	CMRR	*1		45		dB
Operating Current	I_{PGA}			8.67		mA
ACOMP						
Channel				4		
Operation Voltage	V_{DD}		0		V_{DD}	
Input offset voltage	V_{IN_OFFSET}			±10		mV
Output Swing	V_{OUT_SWING}		0.1		V_{DD}-0.1	V

Input Com range	V_{IN_COM}		0.1		V_{DD}-0.1	V
Propagation delay	t_{PROP_DLY}	*1			200	ns
Hysteresis	V_{HYS}			1. 20 mV 2. 40 mV 3. 80mV 4. 120mV		mV
Operating Current	I_{ACOMP}			320		μA
DAC 6 bit						
Output Channel				2		
DAC Bit				6		Bit
Full Code Voltage	V_{RANGE}	V_{ref}=2.5V/4V/V_{DD}		Vref		V
Differential Linearity	DNL	V_{ref}=4V *1	-1		+1	LSB
Integral Non-Linearity	INL	V_{ref}=4V *1	-4		+4	LSB
Linear Range of DAC			10h		F0h	Hex
Settling Time	t_{SETTLE}			5	100	μs
Operating Current	I_{DAC_6B}			137		μA
DAC 10 bit(For Debug)						
Output Channel				1		
DAC Bit				10		Bit
Full Code Voltage	V_{RANGE}	V_{DD}		V_{DD}		V
Differential Linearity	DNL	V_{ref}=4V	-1		+1	LSB
Integral Non-Linearity	INL	V_{ref}=4V	-4		+4	LSB
Linear Range of DAC			10h		F0h	Hex
Settling Time	t_{SETTLE}			5		μs
Operating Current	I_{DAC_6B}			181		μA
Debug Buffer						

Input Offset	V_{IN_OFFSET}			±20		mV
Output Swing	V_{OUT_SWING}		0.2		V_{DD}-0.2	V
Input Swing	V_{IN_SWING}		0.2		V_{DD}-0.2	V
Gain Accuracy				±2		%
Close Loop Gain				1		V/V
DC Gain		*1		80		dB
Bandwidth	BW	*1	6			MHz
Phase Margin	PM	*1		50		degree
Noise	NOISE	*1			650	μVrms
CL	C_L	*1	1.6		50	pF
RL	R_L		1			MΩ
GPIO						
Input low-level voltage	V_{IH}		0.7* V_{DD}			V
Input high-level voltage	V_{IL}				0.3* V_{DD}	V
Output high-level voltage	V_{OH}	V_{DD}=3.3V	V_{DD} -0.4			V
		V_{DD} =5V	0.9* V_{DD}			V
Output low-level voltage	V_{OL}	V_{DD} =3.3V			0.4	V
		V_{DD} =5V			0.1* V_{DD}	V
Pull up resistor	R_{PU}		20		300	KΩ
Pull down resistor	R_{PD}		20		300	KΩ
Input leakage current	I_{LI}			±1		μA
Output leakage current	I_{LO}			±1		μA
Schmitt trigger hysteresis	V_{SMT_HYS}		100			mV
nRST Pin						
Input low-level voltage	V_{IH}		0.7* V_{DD}			V
Input high-level voltage	V_{IL}				0.3* V_{DD}	V
Schmitt trigger	V_{SMT_HYS}		100			mV

hysteresis						
Pull up resistor	R_{PU}		20		300	KΩ
Deglitch Time	$t_{DEGLITCH}$			100		μs
BOOT Pin						
Input low-level voltage	V_{IH}		0.7* V_{DD}			V
Input high-level voltage	V_{IL}				0.3* V_{DD}	V
Schmitt trigger hysteresis	V_{SMT_HYS}		100			mV
Pull down resistor	R_{PD}		20		300	KΩ
Deglitch Time	$t_{DEGLITCH}$			100		μs

Note1. Design by guaranteed.

5. Flash Space

FP5600 is equipped with 64 KB on-chip embedded flash memory as shown in Figure 5-1, which can be updated by Serial Wire Debug (SWD) program. After the chip is powered on, the Cortex®-M0+ CPU gets the code from the Bootloader ROM for fundamental initialization. Security program memory (Security ROM 1) provides user protection for any program code inside the NVR.

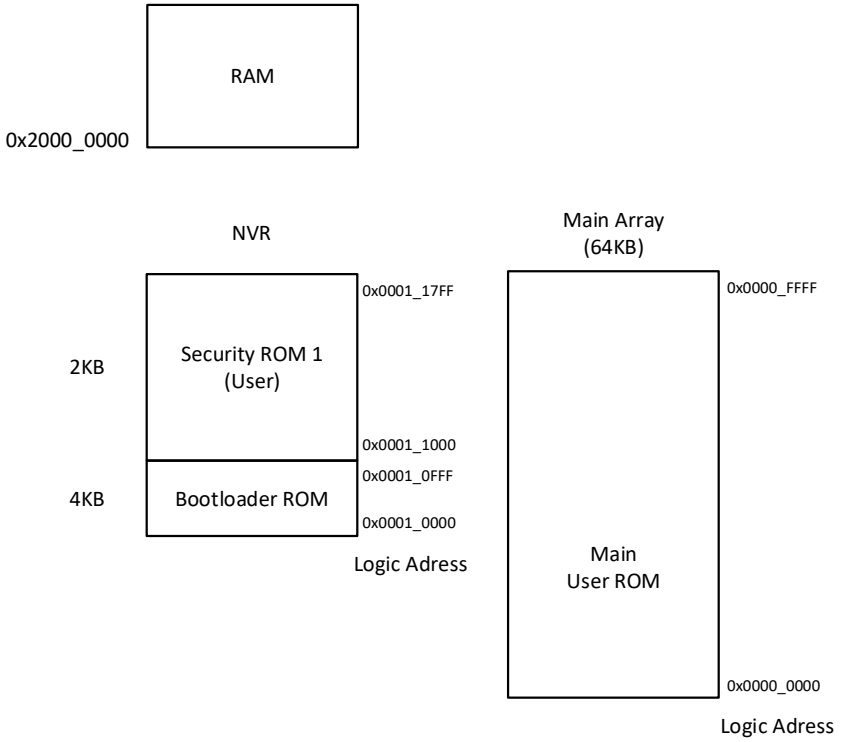


Figure 5-1 Flash Memory Map

6. Register Overview

Index	Module	BUS	Base Address
0	UART0	APB	0x4000_0000
1	UART1	APB	0x4000_0400
2	UART2	APB	0x4000_0800
3			0x4000_0C00
4	SPI0	APB	0x4000_1000
5			0x4000_1400
6			0x4000_1800
7			0x4000_1C00
8	I2C0	APB	0x4000_2000
9			0x4000_2400
10			0x4000_2800
11			0x4000_2C00
12	ADC	APB	0x4000_3000
13			0x4000_3400
14			0x4000_3800
15			0x4000_3C00
16	QEI0	APB	0x4000_4000
17	QEI1	APB	0x4000_4400
18			0x4000_4800
19			0x4000_4C00
20	ETIMER0	APB	0x4000_5000
21	ETIMER1	APB	0x4000_5400
22	ETIMER2	APB	0x4000_5800
23			0x4000_5C00
24	CRC	APB	0x4000_6000
25			0x4000_6400
26			0x4000_6800
27			0x4000_6C00
28	WDT	APB	0x4000_7000
29			0x4000_7400
30			0x4000_7800
31			0x4000_7C00
32	RTC	APB	0x4000_8000
33			0x4000_8400
34			0x4000_8800
35			0x4000_8C00
36	MTPWM0	APB	0x4000_9000
37	MTPWM1	APB	0x4000_9400
38			0x4000_9800
39			0x4000_9C00
40	DMA	APB	0x4000_A000
41			0x4000_A400
42			0x4000_A800
43			0x4000_AC00
44	FMC	APB	0x4000_B000
45			0x4000_B400
46			0x4000_B800
47			0x4000_BC00
48	GLOBAL	APB	0x4000_C000
49			0x4000_C400
50			0x4000_C800
51			0x4000_CC00
52	DUALTIMER0	APB	0x4000_D000
53			0x4000_D400
54			0x4000_D800
55			0x4000_DC00
56	DUALTIMER1	APB	0x4000_E000
57			0x4000_E400
58			0x4000_E800
59			0x4000_EC00
60	ANALOG	APB	0x4000_F000
61	ACOMP	APB	0x4000_F400
62	PGA	APB	0x4000_F800

63			0x4000_FC00
64	CLOCK	AHB	0x5000_0000
65	SYS	AHB	0x5000_1000
66			0x5000_2000
67			0x5000_3000
68			0x5000_4000
69			0x5000_5000
70	GPIOA	AHB	0x5000_6000
71	GPIOB	AHB	0x5000_7000
72	GPIOC	AHB	0x5000_8000
73			0x5000_9000
74			0x5000_A000
75			0x5000_B000
76	CORDIC	AHB	0x5000_C000
77			0x5000_D000
78	HDIV	AHB	0x5000_E000

7. Function Overview

7.1 Universal Asynchronous Receiver/Transmitter (UART)

7.1.1 UART Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	Label
UDATA	0x0000	All		0x00000000	UART Data Register		
	31:12	Reserved	RO	0x0			
	11	OE	RO	0x0	Overrun error	0	NOT_OCCUR
						1	OCCUR
	10	BE	RO	0x0	Break error	0	NOT_OCCUR
						1	OCCUR
	9	PE	RO	0x0	Parity error	0	NOT_OCCUR
						1	OCCUR
	8	FE	RO	0x0	Framing error	0	NOT_OCCUR
						1	OCCUR
	7:0	DATA	RW	0x0	Receive (read) data character. Transmit (write) data character.	(x)	(x)
USTATUS	0x0004	All		0x00000000	UART Status Register		
	31:4	Reserved	RO	0x0			
	3	OE	W1C	0x0	Overrun error	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	BE	W1C	0x0	Break error	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	PE	W1C	0x0	Parity error	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	FE	W1C	0x0	Framing error	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
Reserved	0x0008	All	RO				
	31:0	Reserved	RO	0x0			
UFLG	0x0018	All		0x00000090	UART Flag Register		
	31:9	Reserved	RO	0x0			
	8	RI	RO	0x0	Ring indicator. This bit is the complement of the UART ring	0	

					indicator, nUARTRI, modem status input. That is, the bit is 1 when nUARTRI is LOW.		
						1	
	7	TXFE	RO	0x1	Transmit FIFO empty.	0	NOT_EMPTY
						1	EMPTY
	6	RXFF	RO	0x0	Receive FIFO full.	0	NOT_FULL
						1	FULL
	5	TXFF	RO	0x0	Transmit FIFO full.	0	NOT_FULL
						1	FULL
	4	RXFE	RO	0x1	Receive FIFO empty.	0	NOT_EMPTY
						1	EMPTY
	3	BUSY	RO	0x0	UART busy	0	NOT_BUSY
						1	BUSY
	2	DCD	RO	0x0	Data carrier detect. This bit is the complement of the UART data carrier detect, nUARTDCD, modem status input. That is, the bit is 1 when nUARTDCD is LOW.	0	NOT_OCCUR
						1	OCCUR
	1	DSR	RO	0x0	Data set ready. This bit is the complement of the UART data set ready, nUARTDSR, modem status input. That is, the bit is 1 when nUARTDSR is LOW.	0	NOT_OCCUR
						1	OCCUR
	0	CTS	RO	0x0	Clear to send. This bit is the complement of the UART clear to send, nUARTCTS, modem status input. That is, the bit is 1 when nUARTCTS is LOW.	0	NOT_OCCUR
						1	OCCUR
Reserved	0x001C	All	RO				
	31:0	Reserved	RO	0x0			
LPCNT	0x0020	All		0x00000000	UART Low-Power Counter Register		
	31:8	Reserved	RO	0x0			
	7:0	LPDIV	RW	0x0	8-bit low-power divisor value. These bits are cleared to 0 at reset.	(x)	(x)
BAUD_INTER	0x0024	All		0x00000000	UART Interger Baud Rate Register		
	31:16	Reserved	RO	0x0			
	15:0	INTERDIV	RW	0x0	The integer baud rate divisor. These bits are cleared to 0 on reset.	(x)	(x)
BAUD_FRAC	0x0028	All		0x00000000	UART Fractional Baud Rate Register		
	31:6	Reserved	RO	0x0			
	5:0	FRACDIV	RW	0x0	The fractional baud rate divisor. These bits are cleared to 0 on reset.	(x)	(x)

LINECTL	0x002C	All		0x00000000	UART Line Control Register		
	31:8	Reserved	RO	0x0			
	7	STICK_PARITY	RW	0x0	Stick parity select. This bit has no effect when the LINECTL.PARITY_EN disables parity checking and generation.	0	DISABLE
						1	ENABLE
	6:5	WORD_LENGTH	RW	0x0	Word length.	0	WORD_LENGTH_5_BITS
						1	WORD_LENGTH_6_BITS
						2	WORD_LENGTH_7_BITS
						3	WORD_LENGTH_8_BITS
	4	FIFO_EN	RW	0x0	Enable FIFOs	0	DISABLE
						1	ENABLE
	3	STOPBITS	RW	0x0	Two stop bits select.	0	ONE_STOP_BIT
						1	TWO_STOP_BITS
	2	PARITY_SEL	RW	0x0	Even parity select. This bit has no effect when the LINECTL.PARITY_EN disables parity checking and generation.	0	ODD_PARITY
						1	EVEN_PARITY
	1	PARITY_EN	RW	0x0	Parity enable	0	DISABLE
						1	ENABLE
	0	BREAK	RW	0x0	Send break	0	DISABLE
						1	SEND_BREAK
UCTL	0x0030	All		0x00000300	UART Control Register		
	31:16	Reserved	RO	0x0			
	15	CTS_EN	RW	0x0	CTS hardware flow control enable. Data is only transmitted when the nUARTCTS signal is asserted.	0	DISABLE
						1	ENABLE
	14	RTS_EN	RW	0x0	RTS hardware flow control enable. Data is only requested when there is space in the receive FIFO for it to be received.	0	DISABLE
						1	ENABLE
	13	OUT2	RW	0x0	This bit is the complement of the UART Out2 (nUARTOut2) modem status output. For DTE this can be used as Ring Indicator (RI).	0	OUTPUT_1
						1	OUTPUT_0
	12	OUT1	RW	0x0	This bit is the complement of the UART Out1 (nUARTOut1) modem status output. For DTE this can be used as Data Carrier Detect(DCD).	0	OUTPUT_1
						1	OUTPUT_0
	11	RTS	RW	0x0	Request to send. This bit is the complement of the UART request to send, nUARTRTS, modem status output.	0	NRTS_HIGH
						1	NRTS_LOW
	10	DTR	RW	0x0	Data transmit ready. This bit is the complement of the UART data transmit ready, nUARTDTR, modem status output.	0	NDTR_HIGH
						1	NDTR_LOW

	9	RX_EN	RW	0x1	Receive enable.	0	DISABLE
						1	ENABLE
	8	TX_EN	RW	0x1	Transmit enable.	0	DISABLE
						1	ENABLE
	7	LB_EN	RW	0x0	Loopback enable.	0	DISABLE
						1	ENABLE
	6:3	Reserved	RO	0x0			
	2	SIRLP	RW	0x0	SIR low-power IrDA mode. Setting this bit uses less power, but might reduce transmission distances.	0	PULSE_NARROW
						1	PULSE_WIDE
	1	SIR_EN	RW	0x0	SIR enable	0	DISABLE
						1	ENABLE
	0	UART_EN	RW	0x0	UART enable	0	DISABLE
						1	ENABLE
INTFIFOSEL	0x0034	All		0x00000012	Interrupt FIFO Level Select Register		
	31:6	Reserved	RO	0x0			
	5:3	RXFIFOSEL	RW	0x2	Receive interrupt FIFO level select.	0	FIFO_HIGHER_THAN_1_DIV_8
						1	FIFO_HIGHER_THAN_1_DIV_4
						2	FIFO_HIGHER_THAN_1_DIV_2
						3	FIFO_HIGHER_THAN_3_DIV_4
						4	FIFO_HIGHER_THAN_7_DIV_8
						5	RESERVED
						6	RESERVED
						7	RESERVED
	2:0	TXFIFOSEL	RW	0x2	Transmit interrupt FIFO level select.	0	FIFO_LOWER_THAN_1_DIV_8
						1	FIFO_LOWER_THAN_1_DIV_4
						2	FIFO_LOWER_THAN_1_DIV_2
						3	FIFO_LOWER_THAN_3_DIV_4
						4	FIFO_LOWER_THAN_7_DIV_8
						5	RESERVED
						6	RESERVED
						7	RESERVED
UINTMSK	0x0038	All		0x00000000	Interrupt Mask Set/Clear Register		
	31:11	Reserved	RO	0x0			
	10	OEIM	RW	0x0	Overrun error interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	9	BEIM	RW	0x0	Break error interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	8	PEIM	RW	0x0	Parity error interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	7	FEIM	RW	0x0	Framing error interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	6	RTIM	RW	0x0	Receive timeout interrupt mask.	0	CLEAR_MASK

						1	SET_MASK
	5	TXIM	RW	0x0	Transmit interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	4	RXIM	RW	0x0	Receive interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	3	DSRMIM	RW	0x0	DSR modem interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	2	DCDMIM	RW	0x0	DCD modem interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	1	CTSMIM	RW	0x0	CTS modem interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
	0	RIMIM	RW	0x0	RI modem interrupt mask.	0	CLEAR_MASK
						1	SET_MASK
URAWINTSTS	0x003C	All		0x00000000	Raw Interrupt Status Register		
	31:11	Reserved	RO	0x0			
	10	OERIS	RO	0x0	Overrun error interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	9	BERIS	RO	0x0	Break error interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	8	PERIS	RO	0x0	Parity error interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	7	FERIS	RO	0x0	Framing error interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	6	RTRIS	RO	0x0	Receive timeout interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	5	TXRIS	RO	0x0	Transmit interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	4	RXRIS	RO	0x0	Receive interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	3	DSRRMIS	RO	0x0	DSR modem interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	2	DCDRMIS	RO	0x0	DCD modem interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	1	CTSRMIS	RO	0x0	CTS modem interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	0	RIRMIS	RO	0x0	RI modem interrupt status.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
UMSKINTSTS	0x0040	All		0x00000000	Masked Interrupt Status Register		
	31:11	Reserved	RO	0x0			
	10	OEMIS	RO	0x0	Overrun error masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH

	9	BEMIS	RO	0x0	Break error masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	8	PEMIS	RO	0x0	Parity error masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	7	FEMIS	RO	0x0	Framing error masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	6	RTMIS	RO	0x0	Receive timeout masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	5	TXMIS	RO	0x0	Transmit masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	4	RXMIS	RO	0x0	Receive masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	3	DSRMMIS	RO	0x0	DSR modem masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	2	DCDMMIS	RO	0x0	DCD modem masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	1	CTSMMIS	RO	0x0	CTS modem masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	0	RIMMIS	RO	0x0	RI modem masked interrupt status.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
UINTCLR	0x0044	All		0x00000000	Interrupt Clear Register		
	31:11	Reserved	RO	0x0			
	10	OEIC	W1S	0x0	Overrun error interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	9	BEIC	W1S	0x0	Break error interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	8	PEIC	W1S	0x0	Parity error interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	7	FEIC	W1S	0x0	Framing error interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	6	RTIC	W1S	0x0	Receive timeout interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	5	TXIC	W1S	0x0	Transmit interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	4	RXIC	W1S	0x0	Receive interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	3	DSRMIC	W1S	0x0	DSR modem interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	2	DCDMIC	W1S	0x0	DCD modem interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	1	CTSMIC	W1S	0x0	CTS modem interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	0	RIMIC	W1S	0x0	RI modem interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT

UDMACTL	0x0048	All		0x00000000	DMA Control Register		
	31:3	Reserved	RO	0x0			
	2	DMA_ON_ERROR	RW	0x0	DMA on error.	0	DISABLE
						1	RECEIVE_OUTPUT
	1	TX_DMA_EN	RW	0x0	Transmit DMA enable.	0	DISABLE
						1	ENABLE
	0	RX_DMA_EN	RW	0x0	Receive DMA enable.	0	DISABLE
						1	ENABLE

7.2 Serial Peripheral Interface Bus (SPI)

7.2.1 SPI Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	Label
SPICTL0	0x0000	All		0x00000000	SPI Control 0 Register		
	31:16	Reserved	RO	0x0			
	15:8	CLK_RATE	RW	0x0	Serial clock rate	(x)	ADD_ONE_(x)
	7	PHA	RW	0x0	SPICLKOUT Phase Control Bit	0	AT_FIRST_EDGE
						1	AT_SECOND_EDGE
	6	POL	RW	0x0	SPICLKOUT Polarity Control Bit	0	IDLE_LEVEL_LOW
						1	IDLE_LEVEL_HIGH
	5:4	FRAME_FORMAT	RW	0x0	Frame Format	0	MOTOROLA_FORMAT
						1	TI_FORMAT
						2	NM_FORMAT
						3	RESERVED
	3:0	DATA_SIZE	RW	0x0	Data Size Select	0	RESERVED
						1	RESERVED
						2	RESERVED
						3	4_BIT_DATA
						4	5_BIT_DATA
						5	6_BIT_DATA
						6	7_BIT_DATA
						7	8_BIT_DATA
						8	9_BIT_DATA
						9	10_BIT_DATA
						10	11_BIT_DATA
						11	12_BIT_DATA
						12	13_BIT_DATA
						13	14_BIT_DATA
						14	15_BIT_DATA
						15	16_BIT_DATA
SPICTL1	0x0004	All		0x00000000	SPI Control 1 Register		
	31:4	Reserved	RO	0x0			
	3	SLAVE_OUT	RW	0x0	Slave-mode output disable. This bit is relevant only in the slave mode.	0	SLAVE_OUT_ENABLE
						1	SLAVE_OUT_DISABLE
	2	MODE_SEL	RW	0x0	Master or slave mode select.	0	MASTER_MODE
						1	SLAVE_MODE
	1	SPI_EN	RW	0x0	SPI enable.	0	DISABLE
						1	ENABLE
	0	LB_EN	RW	0x0	Loopback enable.	0	DISABLE
						1	ENABLE
SPIDATA	0x0008	All		0x00000000	SPI Data Register		
	31:16	Reserved	RO	0x0			
	15:0	DATA	RW	0x0	Transmit/Receive FIFO	(x)	(x)
SPISTATUS	0x000C	All		0x00000003	SPI Status Register		
	31:5	Reserved	RO	0x0			

	4	BUSY	RO	0x0	SPI busy	0	NOT_BUSY
						1	BUSY
	3	RFF	RO	0x0	Receive FIFO full.	0	NOT_FULL
						1	FULL
	2	RNE	RO	0x0	Receive FIFO not empty.	0	EMPTY
						1	NOT_EMPTY
	1	TNF	RO	0x1	Transmit FIFO not full.	0	FULL
						1	NOT_FULL
	0	TFE	RO	0x1	Transmit FIFO empty.	0	NOT_EMPTY
						1	EMPTY
SPIDIV	0x0010	All		0x00000000	SPI Clock Prescale Register		
	31:8	Reserved	RO	0x0			
	7:0	SPIDIV	RW	0x0	Clock prescale divisor. Must be an even number from 2-254, depending on the frequency of SPICLK.	(x)	EVEN_(x)
SPI_INTMASK	0x0014	All		0x00000000	SPI Interrupt Mask Register		
	31:4	Reserved	RO	0x0			
	3	TXIM	RW	0x0	Transmit FIFO interrupt mask.	0	SET_INTERRUPT_MASK
						1	CLEAR_INTERRUPT_MASK
	2	RXIM	RW	0x0	Receive FIFO interrupt mask.	0	SET_INTERRUPT_MASK
						1	CLEAR_INTERRUPT_MASK
	1	RTIM	RW	0x0	Receive timeout interrupt mask.	0	SET_INTERRUPT_MASK
						1	CLEAR_INTERRUPT_MASK
	0	RORIM	RW	0x0	Receive overrun interrupt mask.	0	SET_INTERRUPT_MASK
						1	CLEAR_INTERRUPT_MASK
SPI_RAWINTSTS	0x0018	All		0x00000008	SPI Raw Interrupt Status Register		
	31:4	Reserved	RO	0x0			
	3	TXRIS	RO	0x1	Transmit FIFO raw interrupt.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	2	RXRIS	RO	0x0	Receive FIFO raw interrupt.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	1	RTRIS	RO	0x0	Receive timeout raw interrupt.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
	0	RORRIS	RO	0x0	Receive overrun raw interrupt.	0	RAW_INTERRUPT_STATE_LOW
						1	RAW_INTERRUPT_STATE_HIGH
SPI_MSKINTSTS	0x001C	All		0x00000000	SPI Masked Interrupt Status Register		
	31:4	Reserved	RO	0x0			
	3	TXMIS	RO	0x0	Transmit FIFO masked interrupt.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	2	RXMIS	RO	0x0	Receive FIFO masked interrupt.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	1	RTMIS	RO	0x0	Receive timeout masked interrupt.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE_HIGH
	0	RORMIS	RO	0x0	Receive overrun masked interrupt.	0	MASKED_INTERRUPT_STATE_LOW
						1	MASKED_INTERRUPT_STATE

							_HIGH
SPI_INTCLR	0x0020	All		0x00000000	SPI Interrupt Clear Register		
	31:2	Reserved	RO	0x0			
	1	RTIC	W1S	0x0	Receive timeout interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
	0	RORIC	W1S	0x0	Receive overrun interrupt clear.	0	NO_EFFECT
						1	CLEAR_INTERRUPT
SPI_DMACTL	0x0024	All		0x00000000	DMA Control Register		
	31:2	Reserved	RO	0x0			
	1	TX_DMA_EN	RW	0x0	Transmit DMA enable.	0	DISABLE
						1	ENABLE
	0	RX_DMA_EN	RW	0x0	Receive DMA enable.	0	DISABLE
						1	ENABLE

7.3 Inter-Integrated Circuit (I2C)

7.3.1 I2C Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
I2C_TXD	0x0000	All		0x00000000	I2C Data Register: 8-bit transferred data of I2C serial port		
	31:8	Reserved	RO				
	7:0	TX_DATA	RW		I2C Tx Data Register used for the 1. I2C Master Write 2. I2C Slave Read	(x)	(x)
I2C_RXD	0x0004	All		0x00000000	I2C Data Register: 8-bit received data of I2C serial port		
	31:8	Reserved	RO				
	7:0	RX_DATA	RW		I2C Rx Data Register used for the 1. I2C Master Read 2. I2C Slave Write	(x)	(x)
I2C_TXFVALIDCNT	0x0008	All		0x00000000	The amount of the valid elements with TX FIFO, only for DMA Mode		
	31:8	Reserved	RO				
	7:0	VAL	RO		Amount of the valid elements in the FIFO	(x)	(x)
I2C_RxFVALIDCNT	0x000C	All		0x00000000	The amount of the valid elements with RX FIFO, only for DMA Mode		
	31:8	Reserved	RO				
	7:0	VAL	RO		Amount of the valid elements in the FIFO	(x)	(x)
I2C_TXBURSTLEN	0x0010	All		0x00000000	Set the burst length with the master write or slave read, only for DMA Mode (Set by the I2C Master)		
	31:8	Reserved	RO				
	7:0	VAL	RW		transimssion length of the data payload	(x)	(x)
I2C_RXBURSTLEN	0x0014	All		0x00000000	Set the burst length with the master read or slave write, only for DMA Mode (Set by the I2C Master)		
	31:8	Reserved	RO				
	7:0	VAL	RW		transimssion length of the data payload	(x)	(x)
I2C_CTL0	0x0018	All		0x00000000	I2C Control Register		
	31:8	Reserved	RO				
	7	INTEN	RW		Enable Interrupt:new **status code is generated** and stored in I2C_STATUS, the I2C Interrupt	0	DISABLE

					Flag bit SI (I2C_CTL [3]) will be set		
						1	ENABLE
	6	I2CEN	RW		I2C Controller Enable Bit:multi-function pin function must **set to SDA, and SCL**	0	DISABLE
						1	ENABLE
	5	START	RW		I2C START Control:set 1 to **enter Master mode**, the I2C hardware sends a START or repeat START condition to bus when the bus is free	0	DISABLE
						1	ENABLE
	4	STOP	RW		I2C STOP Control: **transmit a STOP condition** to bus then I2C controller will check the bus condition if a STOP condition is detected	0	DISABLE
						1	ENABLE
	3	SI	W1C		I2C **Interrupt Flag**: When a **new I2C state** is present in the I2C_STATUS register, the SI flag is set by hardware. SI must be **cleared by software**. Clear SI by writing 1 to this bit	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	ACK	RW		Assert Acknowledge Control: When ACK=**1** prior to **address or data** is received, an acknowledged (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when 1.). A slave is acknowledging **the address sent from master**, 2.) The receiver devices are acknowledging the **data sent** by transmitter. ACK=**0** prior to address or data received, a **Not acknowledged** (high level to SDA) will be returned during the acknowledge clock pulse on (is slave willing to receive data from master)	0	DISABLE
						1	ENABLE
	1:0	Reserved	RO				
I2C_CTL1	0x001C	All		0x00000000	I2C DMA Control (The Slave and Master must support clock stretching when the I2C DMA mode is enable)		
	31:3	Reserved	RO				
	2	DMARST	W1S		Clear the TX and RX FIFO	0	NO_EFFECT
						1	RESET_DMA
	1	DMARX	RW		1: Enable the I2C DMA RX Function 0: Disable the I2C DMA RX Function	0	DISABLE
						1	ENABLE
	0	DMATX	RW		1: Enable the I2C DMA TX Function 0: Disable the I2C DMA TX Function	0	DISABLE
						1	ENABLE
I2C_STATUS	0x0020	All		0x00000000	I2C Status Register		
	31:8	Reserved	RO				
	7:0	STATUS	RO		I2C Status: The three least significant bits are always 0. The five most significant bits contain the status code. There are 28	(x)	(x)

					possible status codes. When the content of I2C_STATUS is **F8H, no serial interrupt is requested**. Others I2C_STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2C_STATUS one cycle after SI is set by hardware and is still present one cycle after SI has been reset by software. In addition, states **00H stands for a Bus Error**. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.		
I2C_CLKDIV	0x0024	All		0x00000000	I2C Clock Divided Register		
	31:8	Reserved	RO				
	7:0	DIVIDER	RW		I2C Clock Divided Formula: Data Baud Rate of I2C = (system clock) / (4x (I2C_CLKDIV [7:0] +1)). Example: If system clock = 16 MHz, the I2C_CLKDIV [7:0] = 40 (28H), the data baud rate of I2C = 16 MHz/ (4x (40 +1)) = 97.5 Kbits/sec	(x)	(x)
I2C_TIMEOUT	0x0028	All		0x00000000	I2C Time-out Control Register		
	31:3	Reserved					
	2	TOCEN	RW		Time-out Counter Enable Bit When Enabled, the **14-bit time-out counter will start counting when SI is clear**. Setting flag SI to '1' will reset counter and re-start up counting after SI is cleared. 0 = Time-Out Counter Disabled. 1 = Time-Out Counter Enabled.	0 1	DISABLE ENABLE
	1	TOCDIV4	RW		Time-out Counter Input Clock Divided by 4 When Enabled, The **time-out period is extend 4 times.** 0 = Time-Out Counter Input Clock Divided Disabled. 1 = Time-Out Counter Input Clock Divided Enabled.	0 1	DISABLE ENABLE
	0	TO_FLG	W1C		Time-out Flag This bit is set by hardware when **I2C time-out happened** and it can interrupt CPU if I2C interrupt enable bit (INTEN) is set to 1. Note: Software can write 1 to clear this bit.	0 1	NOT_OCCUR OCCUR\WRITE_1_CLEAR
ADDR0	0x002C	All		0x00000000	I2C Slave Address Register 0		
	31:8	Reserved	RO				
	7:1	ADDR			I2C Address: The content of this register is **irrelevant when I2C is in Master mode**. In the slave mode, the seven most significant bits must be loaded with the chip's own	(x)	(x)

					address. The I2C hardware will react if either of the address is matched.		
	0	GENCALL	RW		General Call Function	0	DISABLE
						1	ENABLE
ADDR1	0x0030	All		0x00000000	I2C Slave Address Register 1		
	31:8	Reserved	RO				
	7:1	ADDR			I2C Address: The content of this register is **irrelevant when I2C is in Master mode**. In the slave mode, the seven most significant bits must be loaded with the chip's own address. The I2C hardware will react if either of the address is matched.	(x)	(x)
	0	GENCALL	RW		General Call Function	0	DISABLE
						1	ENABLE
ADDR2	0x0034	All		0x00000000	I2C Slave Address Register 2		
	31:8	Reserved	RO				
	7:1	ADDR			I2C Address: The content of this register is **irrelevant when I2C is in Master mode**. In the slave mode, the seven most significant bits must be loaded with the chip's own address. The I2C hardware will react if either of the address is matched.	(x)	(x)
	0	GENCALL	RW		General Call Function	0	DISABLE
						1	ENABLE
ADDR3	0x0038	All		0x00000000	I2C Slave Address Register 3		
	31:8	Reserved	RO				
	7:1	ADDR			I2C Address: The content of this register is **irrelevant when I2C is in Master mode**. In the slave mode, the seven most significant bits must be loaded with the chip's own address. The I2C hardware will react if either of the address is matched.	(x)	(x)
	0	GENCALL	RW		General Call Function	0	DISABLE
						1	ENABLE
ADDRMSK0	0x003C	All		0x00000000	I2C Slave Address Mask Register: support multiple address recognition with four address mask register		
	31:8	Reserved	RO				
	7:1	ADDRMSK	RW		I2C Address Mask 0 = Mask Disabled (the received corresponding register bit should be exact the same as address register.). 1 = Mask Enabled (the received corresponding address bit is don't care.). I2C bus controllers **support multiple address** recognition with four address mask register. When the bit in the address mask register is set to one, it means **the received corresponding address bit is don't-care**. If the bit is set to zero, that means the received	(x)	(x)

					corresponding register bit should be **exact the same** as address register.		
	0	Reserved	RO				
ADDRMSK1	0x0040	All		0x00000000	I2C Slave Address Mask Register: support multiple address recognition with four address mask register		
	31:8	Reserved	RO				
	7:1	ADDRMSK	RW		I2C Address Mask 0 = Mask Disabled (the received corresponding register bit should be exact the same as address register.). 1 = Mask Enabled (the received corresponding address bit is don't care.). I2C bus controllers **support multiple address** recognition with four address mask register. When the bit in the address mask register is set to one, it means **the received corresponding address bit is don't-care**. If the bit is set to zero, that means the received corresponding register bit should be **exact the same** as address register.	(x)	(x)
	0	Reserved	RO				
ADDRMSK2	0x0044	All		0x00000000	I2C Slave Address Mask Register: support multiple address recognition with four address mask register		
	31:8	Reserved	RO				
	7:1	ADDRMSK	RW		I2C Address Mask 0 = Mask Disabled (the received corresponding register bit should be exact the same as address register.). 1 = Mask Enabled (the received corresponding address bit is don't care.). I2C bus controllers **support multiple address** recognition with four address mask register. When the bit in the address mask register is set to one, it means **the received corresponding address bit is don't-care**. If the bit is set to zero, that means the received corresponding register bit should be **exact the same** as address register.	(x)	(x)
	0	Reserved	RO				
ADDRMSK3	0x0048	All		0x00000000	I2C Slave Address Mask Register: support multiple address recognition with four address mask register		
	31:8	Reserved	RO				
	7:1	ADDRMSK	RW		I2C Address Mask 0 = Mask Disabled (the received corresponding register bit should be exact the same as address register.).	(x)	(x)

					1 = Mask Enabled (the received corresponding address bit is don't care.). I2C bus controllers **support multiple address** recognition with four address mask register. When the bit in the address mask register is set to one, it means **the received corresponding address bit is don't-care**. If the bit is set to zero, that means the received corresponding register bit should be **exact the same** as address register.		
	0	Reserved	RO				

7.4 Analog-to-Digital Converter (ADC)

As shown in Figure 7-1, the ADC system includes ADC front-end, ADC engine, ADC reference, as well as other analog supporting circuits. Digital circuits include ADC sample and convert programmable logic, ROUTEx configuration control, result registers, ADC interrupt logic, interface to device peripheral bus, and interface to other on-chip modules.

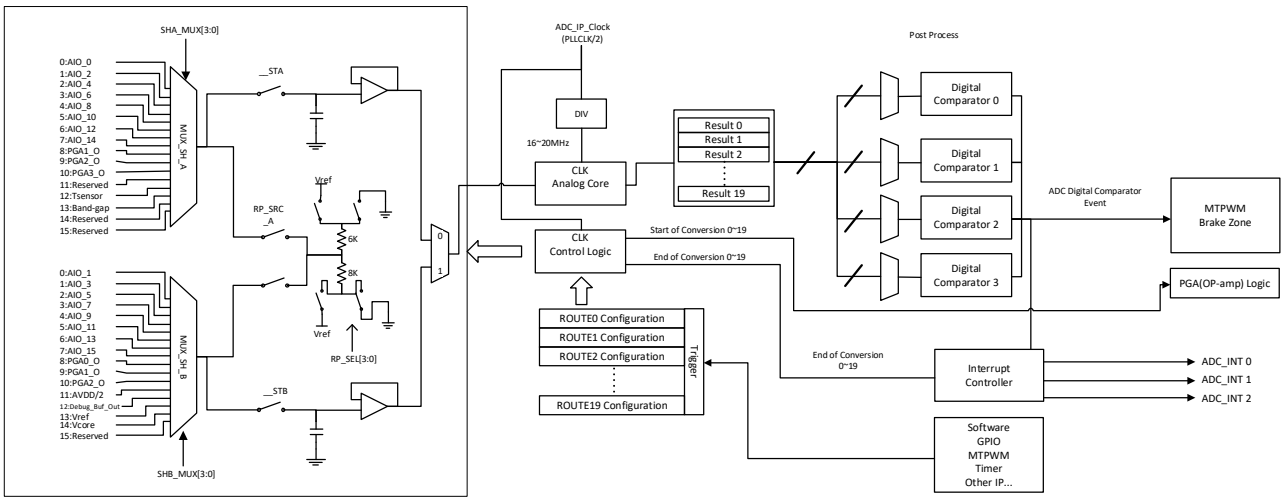


Figure 7-1 ADC Block Diagram

ROUTE can be regarded as a virtual ADC channel. Each virtual channel can be set to correspond to a physical ADC channel. The control logic needs to automatically transfer the MUX of the ADC core to the set channel after a given trigger, and according to the set timing sampling, FP5600 built-in 20 ROUTEs, each virtual channel ROUTEx can be set:

(1) There is an independent trigger source. (Trigger Source)

(2) Target ROUTE channel configuration.

(3) Sampling window time configuration. (Sample-Hold Window)

(4) And there are corresponding independent conversion results. (RESULT register)

(5) Independent interrupt trigger signal (ROUTEx INT Trigger)

Different ROUTEs can correspond to the same channel, which can be used as over sampling at this time. Different ROUTEs can be configured with the same trigger source. When a trigger event occurs, ROUTE will convert according to the set priority level.

FP5600 has two Sample and Hold circuits. The analog core supports simultaneous sampling. In the control logic, ROUTE0/1 or ROUTE4/5 is forced to be bound as a synchronous sampling pair. When synchronous sampling is enabled, the configuration of the ROUTEs is all configured with the even numbered ROUTE as the master.

7.4.1 ADC Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
ADCCTL0	0x0000	All	Protect	0x00000000	ADC Control Register 0.		
	31:1	Reserved	RO	0x0			
	0	EN	RW	0x0	ADC Enable When ADC Disable, ADC will clear all state machine's data.	0	DISABLE
						1	ENABLE
ADCCTL1	0x0004	All	Protect	0x00000000	ADC Control Register 1		
	31:9	Reserved	RO	0x0			
	8	EARLY_INT	RW	0x0	Early interrupt enable This bit control the interrupt timing at the end of ROUTEx conversion or end of sample and hold window.	0	DISABLE
						1	ENABLE
	7	EARLY_ROUTE	RW	0x0	Early sample enable	0	DISABLE
						1	ENABLE
	6	CSTART_CLK	RW	0x0	Configure clock number of C_START signal.	0	C_START_AS_3_CLOCK
						1	C_START_AS_4_CLOCK
	5:0	COREDIV	RW	0x0	ADC core clock divider, it is divided from ADC system clock which general with speed more than 72MHz.	(x)	(x)

ADCCTL2	0x0008	All	Protect	0x00000000	ADC Control Register 2 is designed for open short detection		
	31:30	Reserved	RO	0x0			
	29	CORESEL	RW	0x0	ADC core signal CSTART, SHA, SHB are controlled by ROUTEx logic or ADCCTL2.	0	CONTROL_BY_ROUTE_LOGIC
						1	CONTROL_BY_ADCCTL
	28	CSTART	RW	0x0	Core start control bit	0	SET_LOW
						1	SET_HIGH
	27	STB	RW	0x0	Sample and hold B control bit	0	SET_LOW
						1	SET_HIGH
	26	STA	RW	0x0	Sample and hold A control bit	0	SET_LOW
						1	SET_HIGH
	25	MUXSEL	RW	0x0	ADC core MUX selection control bit field	0	CONTROL_BY_ROUTE_LOGIC
						1	CONTROL_BY_ADCCTL
	24	CHSEL	RW	0x0	Core channel selection bit	0	SHA
						1	SHB
	23:20	MUXSHB	RW	0x0	Select channel to positive terminal of SHB.	0	AIO_1
						1	AIO_3
						2	AIO_5
						3	AIO_7
						4	AIO_9
						5	AIO_11
						6	AIO_13
						7	AIO_15
						8	PGA0_O
						9	PGA1_O
						10	PGA2_O
						11	AVDD_OVER_2
						12	DEBUG_BUF_OUT
						13	VREF

						14	VCORE
						15	RESERVED
	19:16	MUXSHA	RW	0x0	Select channel to positive terminal of SHA.	0	AIO_0
						1	AIO_2
						2	AIO_4
						3	AIO_6
						4	AIO_8
						5	AIO_10
						6	AIO_12
						7	AIO_14
						8	PGA1_O
						9	PGA2_O
						10	PGA3_O
						11	RESERVED
						12	T_SENSOR
						13	BAND_GAP
						14	RESERVED
						15	RESERVED
	15:6	Reserved	RO	0x0			
	5	R8KL	RW	0x0	8K Ohm resistor tie low selection	0	SET_LOW
						1	SET_HIGH
	4	R8KH	RW	0x0	8K Ohm resistor tie high selection	0	SET_LOW
						1	SET_HIGH
	3	R6KL	RW	0x0	6K Ohm resistor tie low selection	0	SET_LOW
						1	SET_HIGH
	2	R6KH	RW	0x0	6K Ohm resistor tie high selection	0	SET_LOW
						1	SET_HIGH
	1	RP_SRC_B	RW	0x0	Open short detection register network enable for SHB	0	DISABLE
						1	ENABLE
	0	RP_SRC_A	RW	0x0	Open short detection register network enable for SHA	0	DISABLE

						1	ENABLE
Reserved	0x000C	All		0x00000000			
	31:0	Reserved	RO	0x0			
ADCINTFLG	0x0010	All		0x00000000	ADC Interrupt Flag Register		
	31:16	Reserved	RO	0x0			
	2	INT2	W1C	0x0	Flag signal indicates if ADC Interrupt 2 is generated	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	INT1	W1C	0x0	Flag signal indicates if ADC Interrupt 1 is generated	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	INT0	W1C	0x0	Flag signal indicates if ADC Interrupt 0 is generated	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
Reserved	0x0014	All		0x00000000			
	31:0	Reserved	RO	0x0			
ADCINTOVFFLG	0x0018	All		0x00000000	ADC Interrupt Overflow Flag Clear Register		
	31:16	Reserved	RO	0x0			
	2	INT2	W1C	0x0	ADC Interrupt 2 overflow flag, write 1 to clear bit	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	INT1	W1C	0x0	ADC Interrupt 1 overflow flag, write 1 to clear bit	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	INT0	W1C	0x0	ADC Interrupt 0 overflow flag, write 1 to clear bit	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
ADCINT0CTL	0x001C	All		0x00000000	ADC Interrupt 0 Control Register		
	31:24	Reserved	RO	0x0			
	23	DICOMP3_LO_EN	RW	0x0	Digital comparator 3 too Low generate interrupt 0 enable. Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE

22	DICOMP3_HI_EN	RW	0x0	Digital comparator 3 too High generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
21	DICOMP2_LO_EN	RW	0x0	Digital comparator 2 too Low generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
20	DICOMP2_HI_EN	RW	0x0	Digital comparator 2 too High generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
19	DICOMP1_LO_EN	RW	0x0	Digital comparator 1 too Low generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
18	DICOMP1_HI_EN	RW	0x0	Digital comparator 1 too High generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
17	DICOMP0_LO_EN	RW	0x0	Digital comparator 0 too Low generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
16	DICOMP0_HI_EN	RW	0x0	Digital comparator 0 too High generate interrupt 0 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE

						1	ENABLE
	15:8	Reserved	RO	0x0			
	7	INTCONTI	RW	0x0	ADC interrupt 1 continuous mode enable	0	CONTINUE_MODE_DISABLE
						1	CONTINUE_MODE_ENABLE
	6	INTEN	RW	0x0	ADC interrupt 1 enable	0	DISABLE
						1	ENABLE
	5	ROUTEEN	RW	0x0	End of ROUTEx conversion generate interrupt pulse	0	DISABLE
						1	ENABLE
	4:0	ROUTESRC	RW	0x0	Select ADC interrupt 0 source which comes from end conversion of ROUTEx.	(x)	(x)
ADCINT1CTL	0x0020	All		0x00000000	ADC interrupt 1 Control Register		
	31:24	Reserved	RO	0x0			
	23	DICOMP3_LO_EN	RW	0x0	Digital comparator 3 too Low generate interrupt 1 enable. Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	22	DICOMP3_HI_EN	RW	0x0	Digital comparator 3 too High generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	21	DICOMP2_LO_EN	RW	0x0	Digital comparator 2 too Low generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	20	DICOMP2_HI_EN	RW	0x0	Digital comparator 2 too High generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE

	19	DICOMP1_LO_EN	RW	0x0	Digital comparator 1 too Low generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	18	DICOMP1_HI_EN	RW	0x0	Digital comparator 1 too High generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	17	DICOMP0_LO_EN	RW	0x0	Digital comparator 0 too Low generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	16	DICOMP0_HI_EN	RW	0x0	Digital comparator 0 too High generate interrupt 1 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	15:8	Reserved	RO	0x0			
	7	INTCONTI	RW	0x0	ADC interrupt 1 continuous mode enable	0	CONTINUE_MODE_DISABLE
						1	CONTINUE_MODE_ENABLE
	6	INTEN	RW	0x0	ADC interrupt 1 enable	0	DISABLE
						1	ENABLE
	5	ROUTEEN	RW	0x0	End of ROUTEx conversion generate interrupt pulse	0	DISABLE
						1	ENABLE
	4:0	ROUTESRC	RW	0x0	Select ADC interrupt 1 source which comes from end conversion of ROUTEx.	(x)	(x)
ADCINT2CTL	0x0024	All		0x00000000	ADC interrupt 2 Control Register		
	31:24	Reserved	RO	0x0			

23	DICOMP3_LO_EN	RW	0x0	Digital comparator 3 too Low generate interrupt 2 enable. Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
22	DICOMP3_HI_EN	RW	0x0	Digital comparator 3 too High generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
21	DICOMP2_LO_EN	RW	0x0	Digital comparator 2 too Low generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
20	DICOMP2_HI_EN	RW	0x0	Digital comparator 2 too High generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
19	DICOMP1_LO_EN	RW	0x0	Digital comparator 1 too Low generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
18	DICOMP1_HI_EN	RW	0x0	Digital comparator 1 too High generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
					1	ENABLE
17	DICOMP0_LO_EN	RW	0x0	Digital comparator 0 too Low generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE

						1	ENABLE
	16	DICOMP0_HI_EN	RW	0x0	Digital comparator 0 too High generate interrupt 2 enable Note that further interrupt will NOT generate if corresponding bit in DICOMPFLG is not cleared. This mechanism can prevent interrupt generate in uncontrollable timing.	0	DISABLE
						1	ENABLE
	15:8	Reserved	RO	0x0			
	7	INTCONTI	RW	0x0	ADC interrupt 2 continuous mode enable	0	CONTINUE_MODE_DISABLE
						1	CONTINUE_MODE_ENABLE
	6	INTEN	RW	0x0	ADC interrupt 2 enable	0	DISABLE
						1	ENABLE
	5	ROUTEEN	RW	0x0	End of ROUTEx conversion generate interrupt pulse	0	DISABLE
						1	ENABLE
	4:0	ROUTESRC	RW	0x0	Select ADC interrupt 2 source which comes from end conversion of ROUTEx.	(x)	(x)
ROUTEPRICTL	0x0028	All		0x00001F00	ADC Route Priority Control Register		
	31:13	Reserved	RO	0x0			
	12:8	ROUND_IDX	RO	0x1F	Round Robin Ring Index Holds the latest ROUTEx in Round Ring, and determine the next order of conversion.	0	ROUTE0
						1	ROUTE1
						2	ROUTE2
						3	ROUTE3
						4	ROUTE4
						5	ROUTE5
						6	ROUTE6
						7	ROUTE7
						8	ROUTE8
						9	ROUTE9
						10	ROUTE10
						11	ROUTE11

						12	ROUTE12
						13	ROUTE13
						14	ROUTE14
						15	ROUTE15
						16	ROUTE16
						17	ROUTE17
						18	ROUTE18
						19	ROUTE19
						20	Reserved
						21	Reserved
						22	Reserved
						23	Reserved
						24	Reserved
						25	Reserved
						26	Reserved
						27	Reserved
						28	Reserved
						29	Reserved
						30	Reserved
						31	RESET_VALUE
	7:6	Reserved	RO	0x0			
	5	PRIORITY_EN	RW	0x0	Priority mode enable.	0	DISABLE
						1	ENABLE
	4:0	PRIORITY	RW	0x0	ROUTE (State-machine of Conversion) Priority Determineds the cutoff point for priority mode and round arbitration of ROUTEs	0	GROUP_ROUTE0_TO_ROUTE0
						1	GROUP_ROUTE0_TO_ROUTE1
						2	GROUP_ROUTE0_TO_ROUTE2
						3	GROUP_ROUTE0_TO_ROUTE3

						4	GROUP_ROUTE0_TO_ROUTE4
						5	GROUP_ROUTE0_TO_ROUTE5
						6	GROUP_ROUTE0_TO_ROUTE6
						7	GROUP_ROUTE0_TO_ROUTE7
						8	GROUP_ROUTE0_TO_ROUTE8
						9	GROUP_ROUTE0_TO_ROUTE9
						10	GROUP_ROUTE0_TO_ROUTE10
						11	GROUP_ROUTE0_TO_ROUTE11
						12	GROUP_ROUTE0_TO_ROUTE12
						13	GROUP_ROUTE0_TO_ROUTE13
						14	GROUP_ROUTE0_TO_ROUTE14
						15	GROUP_ROUTE0_TO_ROUTE15
						16	GROUP_ROUTE0_TO_ROUTE16
						17	GROUP_ROUTE0_TO_ROUTE17
						18	GROUP_ROUTE0_TO_ROUTE18
						19	GROUP_ROUTE0_TO_ROUTE19
						20	Reserved
						21	Reserved
						22	Reserved
						23	Reserved
						24	Reserved
						25	Reserved
						26	Reserved
						27	Reserved
						28	Reserved
						29	Reserved
						30	Reserved
						31	Reserved
ROUTESWTRIG	0x002C	All		0x00000000	Software Trigger ROUTE Register		
	31:16	Reserved	RO	0x0			

19	ROUTE19	W1S	0x0	ROUTEx (State-machine of Conversion) Force Flag. This can be used to initialize a software initiated conversion. If ADCROUTEFLG Register receive both a request to set from software and a request to clear from hardware simultaneously, then software has priority and ADCROUTEFLG will be set.	0	NO_EFFECT
					1	FORCE_CONVERT
18	ROUTE18	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
17	ROUTE17	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
16	ROUTE16	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
15	ROUTE15	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
14	ROUTE14	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
13	ROUTE13	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
12	ROUTE12	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
11	ROUTE11	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
10	ROUTE10	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
9	ROUTE9	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
8	ROUTE8	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
7	ROUTE7	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
					1	FORCE_CONVERT
6	ROUTE6	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT

						1	FORCE_CONVERT
	5	ROUTE5	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
	4	ROUTE4	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
	3	ROUTE3	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
	2	ROUTE2	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
	1	ROUTE1	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
	0	ROUTE0	W1S	0x0	/SAME_AS_BIT_19	0	NO_EFFECT
						1	FORCE_CONVERT
TRIGSTS	0x0030	All		0x00000000	ADC ROUTE Trigger Status Register		
	31:20	Reserved	RO	0x0			
	19	ROUTE19	RO	0x0	ROUTEx (State-machine of Conversion) Flag. This indicates state of each ROUTEx. This bit will be automatically cleared when respective ROUTEx conversion is starting. If this bit receive both a request to set and a request to clear simultaneously, the bit will be set and ignore the request to clear. In this case, the overflow bit in the ADCROUTEOVF Register will not be affected regardless of whether this bit was previously set or not.	0	TRIG_NOT_RECEVIED
						1	TRIG_RECEIVED
	18	ROUTE18	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
						1	TRIG_RECEIVED
	17	ROUTE17	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
						1	TRIG_RECEIVED
	16	ROUTE16	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
						1	TRIG_RECEIVED
	15	ROUTE15	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED

					1	TRIG_RECEIVED
14	ROUTE14	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
13	ROUTE13	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
12	ROUTE12	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
11	ROUTE11	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
10	ROUTE10	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
9	ROUTE9	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
8	ROUTE8	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
7	ROUTE7	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
6	ROUTE6	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
5	ROUTE5	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
4	ROUTE4	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
3	ROUTE3	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
2	ROUTE2	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
1	ROUTE1	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED
					1	TRIG_RECEIVED
0	ROUTE0	RO	0x0	/SAME_AS_BIT_19	0	TRIG_NOT_RECEVIED

						1	TRIG_RECEIVED
TRIGOVFFLG	0x0034	All		0x00000000	ADC ROUTE Trigger Overflow Register		
	31:16	Reserved	RO	0x0			
	19	ROUTE19	W1C	0x0	ROUTEx trigger signal Overflow Flag. When ROUTEx has got a new trig signal and before it finish the current conversion. This bit will be set. It just show that a trigger was missed.	0	NOT_OCCUR
						1	OCCUR
	18	ROUTE18	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	17	ROUTE17	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	16	ROUTE16	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	15	ROUTE15	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	14	ROUTE14	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	13	ROUTE13	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	12	ROUTE12	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	11	ROUTE11	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	10	ROUTE10	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	9	ROUTE9	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	ROUTE8	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7	ROUTE7	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR

						1	OCCUR\WRITE_1_CLEAR
	6	ROUTE6	W1C	0x0	/SAME_AS_BIT_19	0	OVF_NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	5	ROUTE5	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	4	ROUTE4	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	3	ROUTE3	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	ROUTE2	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	ROUTE1	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR
	0	ROUTE0	W1C	0x0	/SAME_AS_BIT_19	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
DATRDYFLG	0x0038	All		0x00000000	ADC ROUTE data ready flag register(latched)		
	31:16	Reserved	RO	0x0			
	19	ROUTE19	W1C	0x0	When ROUTEx finish its conversion and data is latched in corresponding register, this bit is set. This bit is cleared by writing 1.	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	18	ROUTE18	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	17	ROUTE17	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	16	ROUTE16	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	15	ROUTE15	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	14	ROUTE14	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY

	13	ROUTE13	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	12	ROUTE12	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	11	ROUTE11	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	10	ROUTE10	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	9	ROUTE9	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	8	ROUTE8	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	7	ROUTE7	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	6	ROUTE6	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	5	ROUTE5	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	4	ROUTE4	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	3	ROUTE3	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	2	ROUTE2	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	1	ROUTE1	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
	0	ROUTE0	W1C	0x0	/SAME_AS_BIT_19	0	DATA_IS_NOT_READY
						1	DATA_IS_READY
SIMULEN	0x003C	All		0x00000000	ROUTE simultaneous sample enable register		
	31:16	Reserved	RO	0x0			

	9	SIMUL18EN	RW	0x0	Enable simultaneous for ROUTE18/ROUTE19. In this mode, ROUTE19 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE18. That is, trigger of ROUTE19 will be ignored too. Note 1: This bit cannot be set when ROUTE18/ROUTE19 is converting. Note 2: Channel selection of ROUTE19 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE19 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_18_AND_19_SIMUL
						1	ENABLE_ROUTE_18_AND_19_SIMUL
	8	SIMUL16EN	RW	0x0	Enable simultaneous for ROUTE16/ROUTE17. In this mode, ROUTE17 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE16. That is, trigger of ROUTE17 will be ignored too. Note 1: This bit cannot be set when ROUTE16/ROUTE17 is converting. Note 2: Channel selection of ROUTE17 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE17 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_16_AND_17_SIMUL
						1	ENABLE_ROUTE_16_AND_17_SIMUL

	7	SIMUL14EN	RW	0x0	Enable simultaneous for ROUTE14/ROUTE15. In this mode, ROUTE15 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE14. That is, trigger of ROUTE15 will be ignored too. Note 1: This bit cannot be set when ROUTE14/ROUTE15 is converting. Note 2: Channel selection of ROUTE15 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE15 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_14_AND_15_SIMUL
						1	ENABLE_ROUTE_14_AND_15_SIMUL
	6	SIMUL12EN	RW	0x0	Enable simultaneous for ROUTE12/ROUTE13. In this mode, ROUTE13 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE12. That is, trigger of ROUTE13 will be ignored too. Note 1: This bit cannot be set when ROUTE12/ROUTE13 is converting. Note 2: Channel selection of ROUTE13 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE13 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_12_AND_13_SIMUL
						1	ENABLE_ROUTE_12_AND_13_SIMUL

	5	SIMUL10EN	RW	0x0	Enable simultaneous for ROUTE10/ROUTE11. In this mode, ROUTE1 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE10. That is, trigger of ROUTE11 will be ignored too. Note 1: This bit cannot be set when ROUTE10/ROUTE11 is converting. Note 2: Channel selection of ROUTE11 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE11 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_10_AND_11_SIMUL
						1	ENABLE_ROUTE_10_AND_11_SIMUL
	4	SIMUL8EN	RW	0x0	Enable simultaneous for ROUTE8/ROUTE9. In this mode, ROUTE9 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE8. That is, trigger of ROUTE9 will be ignored too. Note 1: This bit cannot be set when ROUTE8/ROUTE9 is converting. Note 2: Channel selection of ROUTE9 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE9 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_8_AND_9_SIMUL
						1	ENABLE_ROUTE_8_AND_9_SIMUL

	3	SIMUL6EN	RW	0x0	Enable simultaneous for ROUTE6/ROUTE7. In this mode, ROUTE7 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE6. That is, trigger of ROUTE7 will be ignored too. Note 1: This bit cannot be set when ROUTE6/ROUTE7 is converting. Note 2: Channel selection of ROUTE7 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE7 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_6_AND_7_SIMUL
						1	ENABLE_ROUTE_6_AND_7_SIMUL
	2	SIMUL4EN	RW	0x0	Enable simultaneous for ROUTE4/ROUTE5. In this mode, ROUTE4 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE4. That is, trigger of ROUTE5 will be ignored too. Note 1: This bit cannot be set when ROUTE4/ROUTE5 is converting. Note 2: Channel selection of ROUTE5 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE19 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_4_AND_5_SIMUL
						1	ENABLE_ROUTE_4_AND_5_SIMUL

	1	SIMUL2EN	RW	0x0	Enable simultaneous for ROUTE2/ROUTE3. In this mode, ROUTE3 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE2. That is, trigger of ROUTE3 will be ignored too. Note 1: This bit cannot be set when ROUTE2/ROUTE3 is converting. Note 2: Channel selection of ROUTE3 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE3 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_2_AND_3_SIMUL
						1	ENABLE_ROUTE_2_AND_3_SIMUL
	0	SIMUL0EN	RW	0x0	Enable simultaneous for ROUTE0/ROUTE1. In this mode, ROUTE0 only provides the channel selection, the sample and hold window (start width) and trigger source are controlled by ROUTE1. That is, trigger of ROUTE1 will be ignored too. Note 1: This bit cannot be set when ROUTE0/ROUTE1 is converting. Note 2: Channel selection of ROUTE1 will be forced at Sample and Hold group B channel. That is, the bit 5 of channel selection bit field of ROUTE1 will be forced in logic 1 in simultaneous mode.	0	DISABLE_ROUTE_0_AND_1_SIMUL
						1	ENABLE_ROUTE_0_AND_1_SIMUL
ROUTE0CTL	0x0050	All		0x00000000	ADC ROUTE0 Control Register		
	31:24	Reserved	RO	0x0			
	23:16	ST_WIDTH	RW	0x0	Select Sample Window Width(unit is ADC core clock).	(x)	(x)
	15:13	Reserved	RO	0x0			

	12:8	TRIGSEL	RW	0x0	Select SMP0 Trigger Source Configures which trigger source will set ROUTE0 flag in the ADCROUTEFLG Register. The Flag will initiate a conversion to start once and the priority is given to ROUTE0. This setting can be overridden by the respective ROUTE0 Field in the ADCINTROUTESEL0~2 Registers.	0	SOFTWARE
						1	ETIMER0_INT
						2	ETIMER1_INT
						3	ETIMER2_INT
						4	QEI0_EVT
						5	QEI1_EVT
						6	INTERNAL_SIGNAL_0
						7	INTERNAL_SIGNAL_1
						8	Reserved
						9	Reserved
						10	MTPWM0_INT
						11	MTPWM0_TRIG0
						12	MTPWM0_TRIG1
						13	MTPWM0_TRIG2
						14	Reserved
						15	MTPWM1_INT
						16	MTPWM1_TRIG0
						17	MTPWM1_TRIG1
						18	MTPWM1_TRIG2
						19	Reserved
						20	ADCINT0
						21	ADCINT1
						22	ADCINT2
						23	Reserved
						24	Reserved
						25	Reserved

						26	Reserved
						27	Reserved
						28	Reserved
						29	Reserved
						30	Reserved
						31	Reserved
	7:5	Reserved	RO				
	4:0	CHSEL	RW	0x0	Select channel of ROUTE, note that Bit4 indicate the selection of Sample Hold A or B.	0	SHA_AIO_0
						1	SHA_AIO_2
						2	SHA_AIO_4
						3	SHA_AIO_6
						4	SHA_AIO_8
						5	SHA_AIO_10
						6	SHA_AIO_12
						7	SHA_AIO_14
						8	SHA_PGA1_O
						9	SHA_PGA2_O
						10	SHA_PGA3_O
						11	RESERVED
						12	SHA_T_SENSOR
						13	SHA_BAND_GAP
						14	RESERVED
						15	RESERVED
						16	SHB_AIO_1
						17	SHB_AIO_3
						18	SHB_AIO_5
						19	SHB_AIO_7
						20	SHB_AIO_9
						21	SHB_AIO_11
						22	SHB_AIO_13

						23	SHB_AIO_15
						24	SHB_OP_0_OUT
						25	SHB_OP_1_OUT
						26	SHB_OP_2_OUT
						27	SHB_AVDD_OVER_2
						28	SHB_DEBUG_BUF_OUT
						29	SHB_VREF
						30	SHB_VCORE
						31	RESERVED
ROUTE1CTL	0x0054	All		0x00000000	ADC ROUTE1 Control Register		
ROUTE2CTL	0x0058	All		0x00000000	ADC ROUTE2 Control Register		
ROUTE3CTL	0x005C	All		0x00000000	ADC ROUTE3 Control Register		
ROUTE4CTL	0x0060	All		0x00000000	ADC ROUTE4 Control Register		
ROUTE5CTL	0x0064	All		0x00000000	ADC ROUTE5 Control Register		
ROUTE6CTL	0x0068	All		0x00000000	ADC ROUTE6 Control Register		
ROUTE7CTL	0x006C	All		0x00000000	ADC ROUTE7 Control Register		
ROUTE8CTL	0x0070	All		0x00000000	ADC ROUTE8 Control Register		
ROUTE9CTL	0x0074	All		0x00000000	ADC ROUTE9 Control Register		
ROUTE10CTL	0x0078	All		0x00000000	ADC ROUTE10 Control Register		
ROUTE11CTL	0x007C	All		0x00000000	ADC ROUTE11 Control Register		
ROUTE12CTL	0x0080	All		0x00000000	ADC ROUTE12 Control Register		
ROUTE13CTL	0x0084	All		0x00000000	ADC ROUTE13 Control Register		
ROUTE14CTL	0x0088	All		0x00000000	ADC ROUTE14 Control Register		
ROUTE15CTL	0x008C	All		0x00000000	ADC ROUTE15 Control Register		
ROUTE16CTL	0x0090	All		0x00000000	ADC ROUTE16 Control Register		
ROUTE17CTL	0x0094	All		0x00000000	ADC ROUTE17 Control Register		
ROUTE18CTL	0x0098	All		0x00000000	ADC ROUTE18 Control Register		
ROUTE19CTL	0x009C	All		0x00000000	ADC ROUTE19 Control Register		
RESULT0	0x00C0	All		0x00000000	ADC Result Register 0		
	31:12	Reserved	RO	0x0			

	11:0	VAL	RO	0x0	12-bit ADC result. Sequential Sampling Mode After the ADC completes a conversion of an ROUTE0, the digital result is placed in the corresponding ADCRESULT0 Register. Simultaneous Sampling Mode After the ADC completes a conversion of a channel pair, the digital results are found in the corresponding ADC RESULTx and ADCRESULTx+1 registers (assuming x is even). For example, for ROUTE0, the completed results of those conversions will be placed in ADCRESULT0 and ADCRESULT1.		(x)
RESULT1	0x00C4	All		0x00000000	ADC Result Register 1		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT2	0x00C8	All		0x00000000	ADC Result Register 2		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT3	0x00CC	All		0x00000000	ADC Result Register 3		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT4	0x00D0	All		0x00000000	ADC Result Register 4		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT5	0x00D4	All		0x00000000	ADC Result Register 5		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT6	0x00D8	All		0x00000000	ADC Result Register 6		
	31:12	Reserved	RO	0x0			

	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT7	0x00DC	All		0x00000000	ADC Result Register 7		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT8	0x00E0	All		0x00000000	ADC Result Register 8		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT9	0x00E4	All		0x00000000	ADC Result Register 9		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT10	0x00E8	All		0x00000000	ADC Result Register 10		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT11	0x00EC	All		0x00000000	ADC Result Register 11		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT12	0x00F0	All		0x00000000	ADC Result Register 12		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT13	0x00F4	All		0x00000000	ADC Result Register 13		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT14	0x00F8	All		0x00000000	ADC Result Register 14		
	31:12	Reserved	RO	0x0			

	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT15	0x00FC	All		0x00000000	ADC Result Register 15		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT16	0x0100	All		0x00000000	ADC Result Register 16		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT17	0x0104	All		0x00000000	ADC Result Register 17		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT18	0x0108	All		0x00000000	ADC Result Register 18		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
RESULT19	0x010C	All		0x00000000	ADC Result Register 19		
	31:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	12-bit ADC result.		(x)
Reserved	0x0110	All		0x00000000			
	31:0	Reserved	RO	0x0			
DICOMPCTL	0x0120	All		0x00000000	Digital Comparator Control Register		
	31:30	Reserved	RO	0x0			
	29	CMP3_EN	RW	0x0	Enable Digital Comparator 3	0	DISABLE

						1	ENABLE
	28:24	SRC3	RW	0x0	Select ROUTEx result as the source of digital comparator 3 input	(x)	FROM_(x)
	23:21	Reserved	RO	0x0			
	21	CMP2_EN	RW	0x0	Enable Digital Comparator 2	0	DISABLE
						1	ENABLE
	20:16	SRC2	RW	0x0	Select ROUTEx result as the source of digital comparator 2 input	(x)	FROM_(x)
	15:14	Reserved	RO	0x0			
	13	CMP1_EN	RW	0x0	Enable Digital Comparator 1	0	DISABLE
						1	ENABLE
	12:8	SRC1	RW	0x0	Select ROUTEx result as the source of digital comparator 1 input	(x)	FROM_(x)
	7:6	Reserved	RO	0x0			
	5	CMP0_EN	RW	0x0	Enable Digital Comparator 0	0	DISABLE
						1	ENABLE
	4:0	SRC0	RW	0x0	Select ROUTEx result as the source of digital comparator 0 input	(x)	FROM_(x)
DICOMP0	0x0124	All		0x00000000	Threshold value for digital comparator 0		
	31:28	Reserved	RO	0x0			
	27:16	LOW_VAL	RW	0x0	Too low threshold value for digital comparator 0. (12 bit)	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	HIGH_VAL	RW	0x0	Too high threshold value for digital comparator 0. (12 bit)	(x)	(x)
DICOMP1	0x0128	All		0x00000000	Threshold value for digital comparator 1		
	31:28	Reserved	RO	0x0			

	27:16	LOW_VAL	RW	0x0	Too low threshold value for digital comparator 0. (12 bit)	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	HIGH_VAL	RW	0x0	Too high threshold value for digital comparator 0. (12 bit)	(x)	(x)
DICOMP2	0x012C	All		0x00000000	Threshold value for digital comparator 2		
	31:28	Reserved	RO	0x0			
	27:16	LOW_VAL	RW	0x0	Too low threshold value for digital comparator 0. (12 bit)	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	HIGH_VAL	RW	0x0	Too high threshold value for digital comparator 0. (12 bit)	(x)	(x)
DICOMP3	0x0130	All		0x00000000	Threshold value for digital comparator 3		
	31:28	Reserved	RO	0x0			
	27:16	LOW_VAL	RW	0x0	Too low threshold value for digital comparator 0. (12 bit)	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	HIGH_VAL	RW	0x0	Too high threshold value for digital comparator 0. (12 bit)	(x)	(x)
DICOMPFLG	0x0134	All		0x00000000	Output flag of digital comparator		
	31:8	Reserved	RO	0x0			
	7	LO_OUT3	W1C	0x0	The output of digital comparator 3 for low threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	6	HI_OUT3	W1C	0x0	The output of digital comparator 3 for high threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR

	5	LO_OUT2	W1C	0x0	The output of digital comparator 2 for low threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	4	HI_OUT2	W1C	0x0	The output of digital comparator 2 for high threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	3	LO_OUT1	W1C	0x0	The output of digital comparator 1 for low threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	HI_OUT1	W1C	0x0	The output of digital comparator 1 for high threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	LO_OUT0	W1C	0x0	The output of digital comparator 0 for low threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	HI_OUT0	W1C	0x0	The output of digital comparator 0 for high threshold	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
DLYCAP0	0x0140	All		0x00000000	Trigger Delay capture register		
	31:25	Reserved	RO	0x0			
	24	OVF	W1C	0x0	Capture Overflow Flag(Latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	23:17	Reserved	RO	0x0			
	20:16	SRC	RW	0x0	Select ROUTEx to calculate	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	Counter from trig pulse to end of ROUTEx sample and hold.	(x)	(x)
DLYCAP1	0x0144	All		0x00000000	Trigger Delay capture register 1		
	31:25	Reserved	RO	0x0			
	24	OVF	W1C	0x0	Capture Overflow Flag(Latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR

	23:17	Reserved	RO	0x0			
	20:16	SRC	RW	0x0	Select ROUTEx to calculate	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	VAL	RO	0x0	Counter from trig pulse to end of ROUTEx sample and hold.	(x)	(x)
DLYCAP2	0x0148	All		0x00000000	Trigger Delay capture register 2		
	31:25	Reserved	RO	0x0			
	24	OVF	W1C	0x0	Capture Overflow Flag(Latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	23:17	Reserved	RO	0x0			
	20:16	SRC	RW		Select ROUTEx as capture source	(x)	(x)
	15:12	Reserved	RO	0x0			
	11:0	VAL	RO		Counter from trig pulse to end of ROUTEx sample and hold.	(x)	(x)
DLYCAP3	0x014C	All		0x00000000	Trigger Delay capture register 3		
	31:25	Reserved	RO	0x0			
	24	OVF	W1C	0x0	Capture Overflow Flag(Latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	23:17	Reserved	RO	0x0			
	20:16	SRC	RW	0x0	Select ROUTEx to calculate	(x)	(x)
	15:12	Reserved	RO	0x0			

	11:0	VAL	RO	0x0	Counter from trig pulse to end of ROUTEx sample and hold.	(x)	(x)
CALGAIN1	0x0150	All		0x00000000	calibration gain register 1		
	31:16	gain1	RO	0x0	calibration gain 1	(x)	(x)
	15:0	gain2	RO	0x0	calibration gain 2	(x)	(x)
CALGAIN2	0x0154	All		0x00000000	calibration gain register 2		
	31:16	gain3	RO	0x0	calibration gain 3	(x)	(x)
	15:0	gain4	RO	0x0	calibration gain 4	(x)	(x)
CALOFFSET1	0x0158	All		0x00000000	calibration offset register 1		
	31:16	offset1	RO	0x0	calibration offset 1	(x)	(x)
	15:0	offset2	RO	0x0	calibration offset 2	(x)	(x)
CALOFFSET2	0x015C	All		0x00000000	calibration offset register 2		
	31:16	offset3	RO	0x0	calibration offset 3	(x)	(x)
	15:0	offset4	RO	0x0	calibration offset 4	(x)	(x)

7.5 Quadrature Encoder Interface (QEI)

FP5600 contains 2 QEI controllers. Inputs QEIx_A and QEIx_B in the QEI accept outputs from quadrature encoding sources such as incremental optical encoders. Two channels, QEIx_A and QEIx_B, are required, normally 90 degrees out of phase. Quadrature encoders typically provide an index signal (pin IDXx), which can be used to indicate absolute position. The QEI control unit is preceded by a debounce filter and polarity control for each signal.

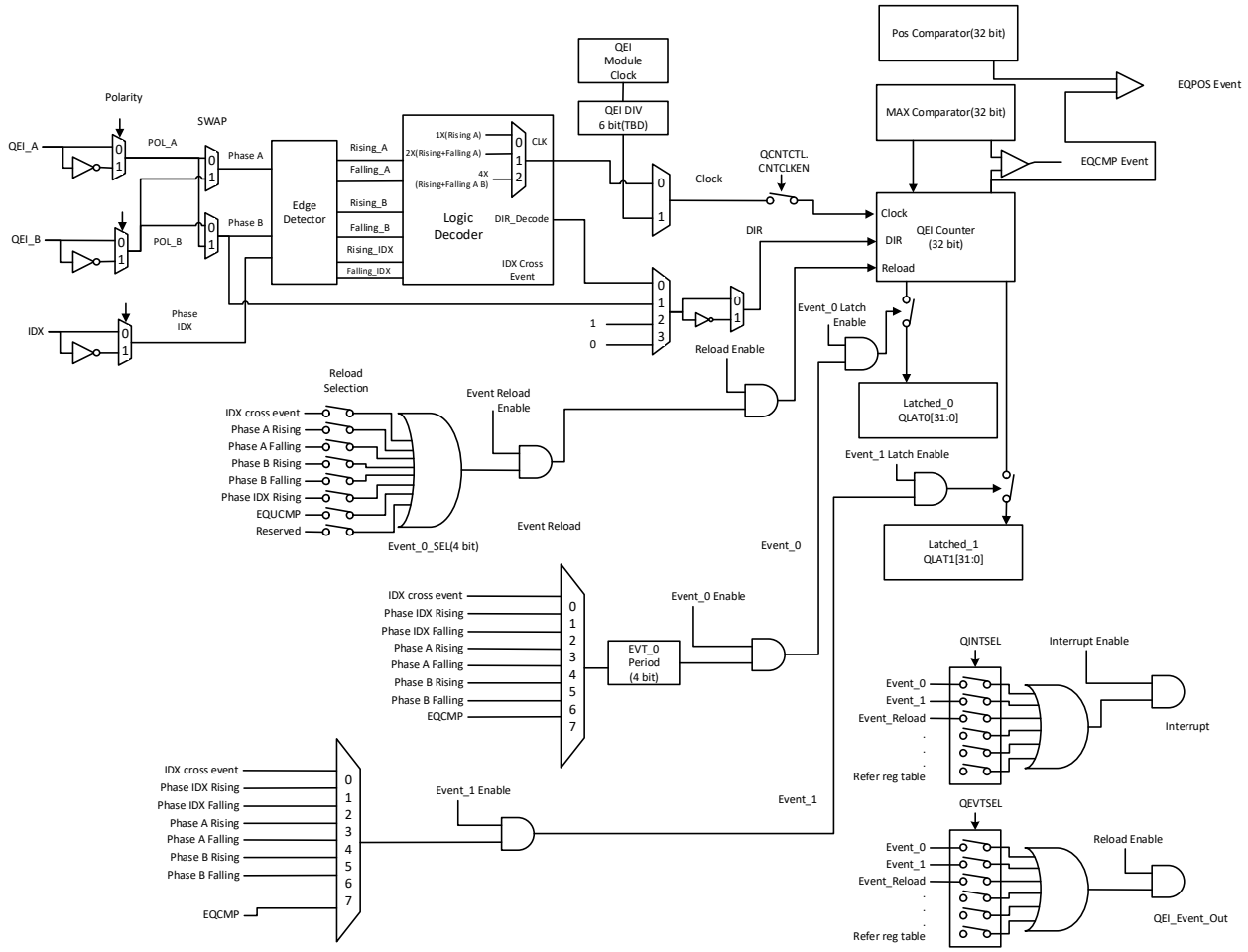


Figure 7-2 QEI block diagram

7.5.1 QEI Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
QEICTL	0x0000	All	Protect	0x00000000	QEI Control Register		
	31:7	Reserved	RO	0x0			
	6:1	QEIDIV	RW	0x0	QEI Divider	(x)	(x)
	0	QEIEN	RW	0x0		0	QEI_DISABLE
						1	QEI_ENABLE
DECCTL	0x0004	All	Protect	0x00000000	QEI Decode Control Register		
	31:9	Reserved	RO	0x0			
	8	IDXRST	W1S	0x0	Reset IDX cross event state when this bit is set. The hardware will auto clear this bit.	0	NO_EFFECT
						1	WERITE_1_RESET
	7:6	CLKMODESEL	RW	0x0	Select QEI clock resolution mode	0	RESOLUTION_1X
						1	RESOLUTION_2X
						2	RESOLUTION_4X
						3	Reserved
	5	Reserved	RO	0x0			

	4	IDXPOL	RW	0x0	Select POL_IDX signal with inverter or not	0	POL_IDX_EQU_IDX
						1	POL_IDX_EQU_NOT_IDX
	3	PBSEL	RW	0x0	Select Phase B comes from A or B after polarity selection	0	PHASE_B_FROM_POL_B
						1	PHASE_B_FROM_POL_A
	2	PASEL	RW	0x0	Select Phase A comes from A or B after polarity selection	0	PHASE_A_FROM_POL_A
						1	PHASE_A_FROM_POL_B
	1	QBPOL	RW	0x0	Select POL_B signal with inverter or not	0	POL_B_EQU_QB
						1	POL_B_EQU_NOT_QB
	0	QAPOL	RW	0x0	Select POL_A signal with inverter or not	0	POL_A_EQU_QA
						1	POL_A_EQU_NOT_QA
QCNTCTL	0x0008	All		0x00000000	QEI multi-function counter control register		
	31:22	Reserved	RO	0x0			
	21	EVT1LATEN	RW	0x0	Latch QEICNT value in QLAT1 when Event 1 occurs.	0	EVENT_1_LATCH_CNT_DISABLE
						1	EVENT_1_LATCH_CNT_ENABLE
	20	EVT0LATEN	RW	0x0	Latch QEICNT value in QLAT0 when Event 0 occurs.	0	EVENT_0_LATCH_CNT_DISABLE
						1	EVENT_0_LATCH_CNT_ENABLE
	19	RLDEN	RW	0x0	Enable/Disable the QEICNT reload when Event reload occurs	0	RELOAD_CNT_DISABLE
						1	RELOAD_CNT_ENABLE
	18	DIRINV	RW	0x0	Invert direction or not	0	DIR_NOT_INVERT
						1	DIR_INVERT
	17:16	DIRSEL	RW	0x0	Select QEICNT counter increase(Up)/decrease(Down) direction	0	FROM_DECODER
						1	FROM_QPHASE_B
						2	FORCE_UP_COUNT
						3	FORCE_DOWN_COUNT
	15:3	Reserved	RO	0x0			
	2	SWRLDEN	W1S	0x0	Software Reload Counter	0	NO_EFFECT
						1	WERITE_1_RELOAD
	1	CNTCLKEN	RW	0x0	QEI Counter clock enable bit	0	DISABLE
						1	ENABLE
	0	CNTCLKSEL	RW	0x0	Clock Source Selection	0	FROM_DECODER

						1	FROM_MODULE_CLK
EVTCTL	0x000C	All		0x00000000	QEI Event_0 and Event_1 control register		
	31:24	Reserved	RO	0x0			
	23:20	EVT1PRD	RW	0x0	QEI Event_0 period select It determines how many selected events need to occur before a trigger pulse is generated.	(x)	(x)
	19:16	EVT1SEL	RW	0x0		0	IDX_CROSS_EVENT
						1	PHASE_IDX_RISING
						2	PHASE_IDX_FALLING
						3	PHASE_A_RISING
						4	PHASE_A_FALLING
						5	PHASE_B_RISING
						6	PHASE_B_FALLING
						7	EQCMP
						8	OTHER_IP
						9	Reserved
						10	Reserved
						11	Reserved
						12	Reserved
						13	Reserved
						14	Reserved
						15	Reserved
	15:13	Reserved	RO	0x0			
	12	EVT1EN			Enable/Disable Event_0 which used as latch trig signal.	0	EVENT_1_DISABLE
						1	EVENT_1_ENABLE
	11:8	EVT0PRD	RW	0x0	QEI Event_0 period select It determines how many selected events need to occur before a trigger pulse is generated.	(x)	(x)
	7:4	EVT0SEL	RW	0x0		0	IDX_CROSS_EVENT
						1	PHASE_IDX_RISING
						2	PHASE_IDX_FALLING
						3	PHASE_A_RISING
						4	PHASE_A_FALLING
						5	PHASE_B_RISING

						6	PHASE_B_FALLING
						7	EQCMP
						8	Reserved
						9	Reserved
						10	Reserved
						11	Reserved
						12	Reserved
						13	Reserved
						14	Reserved
						15	Reserved
	3:1	Reserved	RO	0x0			
	0	EVT0EN			Enable/Disable Event_0 which used as latch trig signal.	0	EVENT_0_DISABLE
						1	EVENT_0_ENABLE
RLDEVTCTL	0x0010	All		0x00000000	QEI reload event control register.		
	31:17	Reserved	RO	0x0			
	16	RLDEN	RW	0x0	QEI module interrupt enable.	0	DISABLE
						1	ENABLE
	15:8	Reserved	RO	0x0			
	7	EQCMP	RW	0x0	Reload event from Phase A rising edge	0	FROM_PHASE_A_RISING_DISABLE
						1	FROM_PHASE_A_RISING_ENABLE
	6	IDXFALL	RW	0x0	Reload event from IDX rising edge	0	FROM_PHASE_A_RISING_DISABLE
						1	FROM_PHASE_A_RISING_ENABLE
	5	IDXRISE	RW	0x0	Reload event from IDX rising edge	0	FROM_PHASE_A_RISING_DISABLE
						1	FROM_PHASE_A_RISING_ENABLE
	4	PHSBFALL	RW	0x0	Reload event from Phase B rising edge	0	FROM_PHASE_B_RISING_DISABLE
						1	FROM_PHASE_B_RISING_ENABLE
	3	PHSBRISE	RW	0x0	Reload event from Phase B rising edge	0	FROM_PHASE_B_RISING_DISABLE
						1	FROM_PHASE_B_RISING_ENABLE
	2	PHSAFALL	RW	0x0	Reload event from Phase A rising edge	0	FROM_PHASE_A_RISING_DISABLE
						1	FROM_PHASE_A_RISING_ENABLE
	1	PHSARISE	RW	0x0	Reload event from Phase A rising edge	0	FROM_PHASE_A_RISING_DISABLE
						1	FROM_PHASE_A_RISING_ENABLE
	0	IDXCROSS	RW	0x0	Reload event from Phase A rising edge	0	FROM_IDX_CROSS_DISABLE
						1	FROM_IDX_CROSS_ENABLE
QEICNT	0x0014	ALL	Protect	0x00000000	QEI multi-function counter		
	31:0	VAL	RO	0x0		(x)	(x)

QLAT0	0x0018	ALL	Protect	0x00000000	QEI latch_0 register		
	31:0	VAL	RO	0x0		(x)	(x)
QLAT1	0x001C	ALL	Protect	0x00000000	QEI latch_1 register		
	31:0	VAL	RO	0x0		(x)	(x)
CMPMAX	0x0020	ALL	Protect	0x00000000	QEI max compare		
	31:0	VAL	RW	0x0		(x)	(x)
QEICNTRLD	0x0024	ALL	Protect	0x00000000	QEI multi-function counter reload register		
	31:0	VAL	RW	0x0	Reload register	(x)	(x)
CMPPOS	0x0028	All		0x00000000	Position compare register		
	31:0	VAL	RW	0x0		(x)	(x)
QINTCTL	0x0040	All		0x00000000	All the bits are OR and final AND with INTEN to generate interrupt signal		
	31:17	Reserved	RO	0x0			
	16	INTEN	RW	0x0	QEI module interrupt enable.	0	DISABLE
						1	ENABLE
	15:7	Reserved	RO	0x0			
	7	EQPOS	RW	0x0		0	DISABLE
						1	ENABLE
	6	IDXCROSS	RW	0x0	Indicate the first IDX cross event occur will generate interrupt	0	DISABLE
						1	ENABLE
	5	DIREX	RW	0x0	Direction exchange will generate interrupt	0	DISABLE
						1	ENABLE
	4	DECERR	RW	0x0	Decoder of QEI error will generate interrupt	0	DISABLE
						1	ENABLE
	3	EQCMP	RW	0x0	Event EQCMP generate the interrupt	0	DISABLE
						1	ENABLE
	2	EVTRLDEN	RW	0x0	Event reload generate interrupt	0	DISABLE
						1	ENABLE
	1	EVT1EN	RW	0x0	Event_1 generate interrupt	0	DISABLE
						1	ENABLE
	0	EVT0EN	RW	0x0	Event_0 reload generate interrupt	0	DISABLE
						1	ENABLE

EVTFLG	0x0044	All		0x00000000	QEI event latched flag register		
	31:27	Reserved	RO	0x0			
	26	DIR_EVT1	W1C	0x0	Latch the direction bit when Event1(Latch) event occurs	0	DIR_IS_DOWN_COUNT
						1	DIR_IS_UP_COUNT\WRITE_1_CLEAR
	25	DIR_EVT0	W1C	0x0	Latch the direction bit when Event0(Latch) event occurs	0	DIR_IS_DOWN_COUNT
						1	DIR_IS_UP_COUNT\WRITE_1_CLEAR
	24	DIR_RLD	W1C	0x0	Latch the direction bit when Reload event occurs	0	DIR_IS_DOWN_COUNT
						1	DIR_IS_UP_COUNT\WRITE_1_CLEAR
	23:22	Reserved	RO	0x0			
	21:20	IDXSTATE	RO	0x0	When decoder catch the first IDX cross event, latch the state of Phase A and Phase B at that moment.	0	IDX_CROSS_WHEN_STATE_0_AND_1
						1	IDX_CROSS_WHEN_STATE_1_AND_2
						2	IDX_CROSS_WHEN_STATE_2_AND_3
						3	IDX_CROSS_WHEN_STATE_3_AND_0
	19:7	Reserved	RO	0x0			
	7	EQPOS	W1C	0x0		0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	6	IDXCROSS	W1C	0x0	Indicate the first IDX cross event occur	0	NOT_OCCUR
						1	FIRST_OCCUR\WRITE_1_CLEAR
	5	DIREX	W1C	0x0	Direction exchange	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	4	DECERR	W1C	0x0	Decoder of QEI error	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	3	EQCMP	W1C	0x0		0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	EVTRLD	W1C	0x0		0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	EVT1	W1C	0x0		0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	EVT0	W1C	0x0		0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
QEISTS	0x0048	All		0x00000000	QEI event status register (Non-Latched)		
	31:4	Reserved	RO	0x0			
	3	IDX	RO	0x0	Reflect IDX value	0	IS_LOW
						1	IS_HIGH
	2	PHB	RO	0x0	Reflect PHB value	0	IS_LOW
						1	IS_HIGH
	1	PHA	RO	0x0	Reflect PHA value	0	IS_LOW
						1	IS_HIGH
	0	DIR	RO	0x0	Indicate direction of counter now	0	COUNTING_DOWN
						1	COUNTING_UP

7.6 Enhanced Timer (ETIMER)

The enhanced timer (ETIMER) module as Figure 7-3, is used in situations where accurate timing of external events is important. This chapter describes the module and how to use it.

Uses for ETIMER include:

(1) Speed measurements of rotating machinery (e.g., e-bike motor with Hall sensors)

(2) Measure period and duty cycle of pulse signals

(3) Decoding information derived from duty cycle encoded systems

The ETIMER module described in this guide includes the following features:

(1) 16-bit time based divider

(2) 4-event time-stamp registers (each 16 bits)

(3) Edge polarity selection for up to four sequenced time-stamp capture events

(4) Interrupt on either of the four events

(5) Single shot capture of up to four event time-stamps

(6) Continuous mode capture of time-stamps in a four-deep circular buffer

(7) Absolute time-stamp capture

(8) Difference (Delta) mode time-stamp capture

(9) All above resources dedicated to a single input pin

The ETIMER module can be configured as a PWM output if not used in capture mode

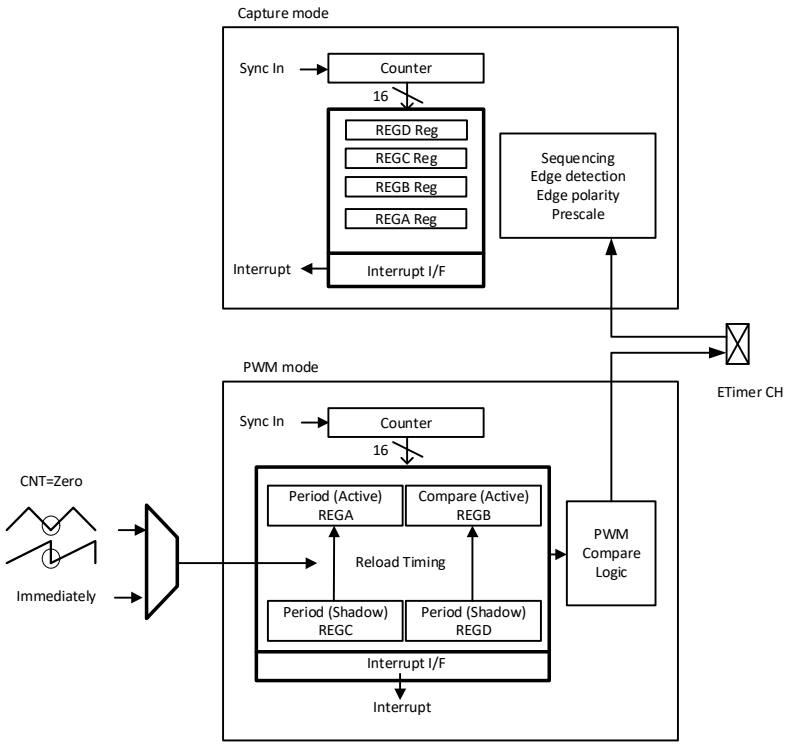


Figure 7-3 Capture and PWM Modes of Operation

User can take ETIMER module resources to implement a single-channel PWM generator (with 16 bit capabilities) when it is not being used for input captures. The counter operates in count-up and up-down mode, providing a time-base for pulse width modulation (PWM) waveforms.

The CAP1 and CAP2 registers become the active period and compare registers, respectively, while CAP3 and CAP4 registers become the period and capture shadow registers, respectively. Figure 7-4 is a high-level view of both the capture and aux pulse-width modulator (PWM) modes of operation.

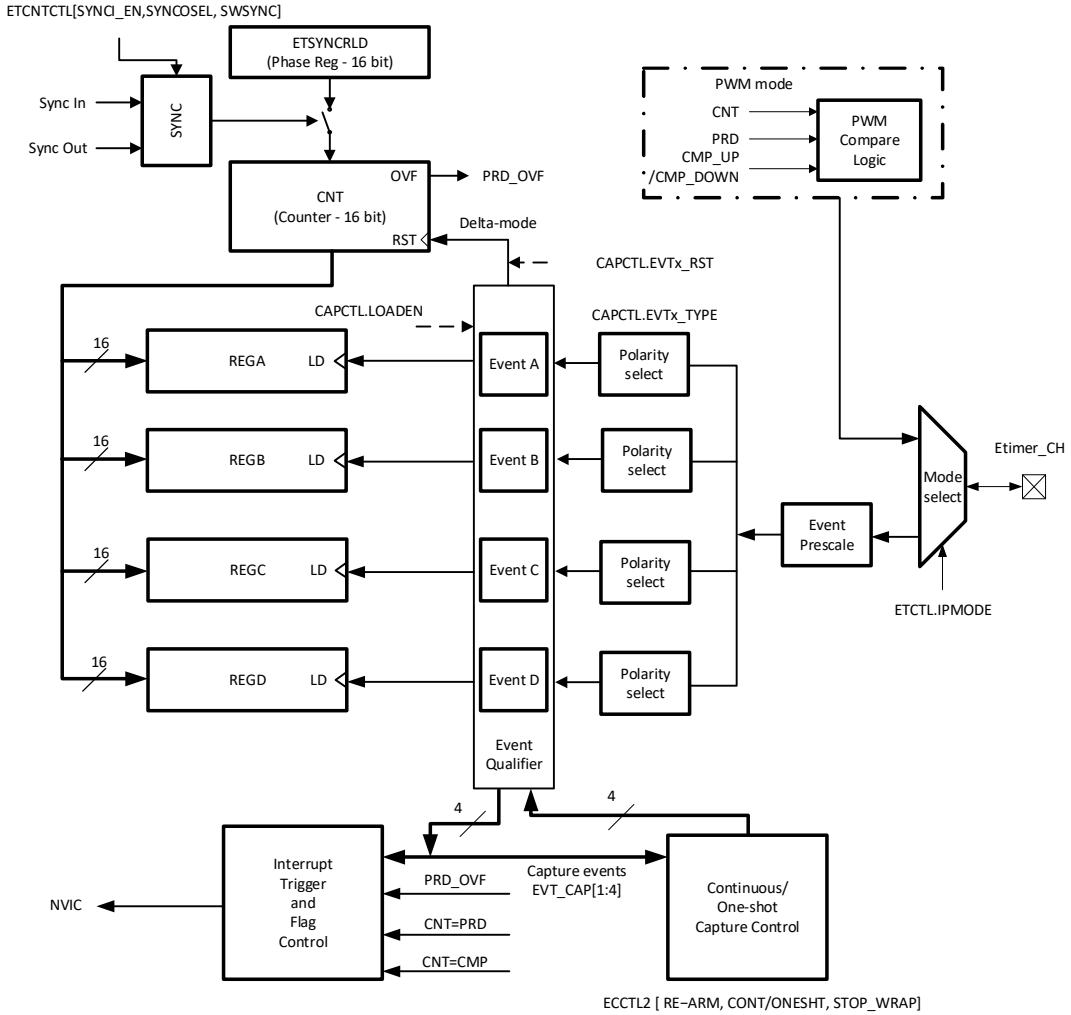


Figure 7-4 Capture Function Diagram

7.3.1 ETIMER Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	Label
ETCTL	0x0000	All		0x00000000	ETIMER Control Register		
	31	BRK_SWTRIG	W1S	0x0	Brake Software Trigger	0	DISABLE
						1	ENABLE
	30:28	Reserved	RO	0x0			
	27:24	BRK_SRC	RW	0x0	Only works in Timer-PWM mode. Brake Source Configuration	0	FROM_ACOMP_0_OUT
						1	FROM_ACOMP_1_OUT

						2	FROM_ACOMP_2_OUT
						3	FROM_ACOMP_3_OUT
						4	INTERNAL_SIGNAL_0
						5	INTERNAL_SIGNAL_1
						6	FROM_DICOMP_0_OUT
						7	FROM_DICOMP_1_OUT
						8	FROM_DICOMP_2_OUT
						9	FROM_DICOMP_3_OUT
						10	RESERVED
						11	RESERVED
						12	RESERVED
						13	RESERVED
						14	RESERVED
						15	RESERVED
	23	BRK_EN	RW	0x0	Brake Enable Bit	0	DISABLE
						1	ENABLE
	22	BRK_STS	W1C	0x0	Brake Status	0	BRAKE_NOT_OCCUR
						1	BRAKE_OCCUR\ WRITE_1 _CLEAR
	21	BRK_POL	RW	0x0	Only works in Timer-PWM mode. Brake source type selection	0	ACTIVE_HIGH
						1	ACTIVE_LOW
	20	BRK_WAV	RW	0x0	Only works in Timer-PWM mode. Action on output PWM final output channel when a brake event occurs. Note that in ETIMERx, brake works as one-shot brake which means the waveform coming back only when CPU clear brake flag in ETFLG.	0	SET_LOW
						1	SET_HIGH
	19:18	Reserved	RO	0x0			
	17	PWM_POL	RW	0x0	Configure PWM output polarity. This bit works only in Timer-PWM mode.	0	NORMAL
						1	INVERTER
	16	PWM_OUTEN	RW	0x0	PWM Output Enable	0	DISABLE
						1	ENABLE
	15:1	Reserved	RO	0x0			
	0	IPMODE	RW	0x0	PWM-Timer or Capture operating mode select	0	PWM_TIMER_MODE
						1	CAPTURE_MODE
ETSAWCTL	0x0004	All	Protect	0x00000000	Enhenced Timer Saw-Wave Control Register		
	31:15	Reserved	RO	0x0			
	14:13	DBGSTOP	RW	0x0	Software emulation mode It define the SAWCNT behavior when CPU hault in debug mode.	0	STOP_AFTER_PERIOD

						1	STOP_AFTER_CLOCK
						2	KEEP_RUN
						3	Reserved
	12:8	FINTNUM	RW	0x0	PWM number(a full period) counter when finite mode(5 bit)	(x)	PERIOD_NUM(x)
	7:3	Reserved	RO	0x0			
	2	TYPE	RW	0x0	Saw-Wave counter period register (SAWPRD) load type	0	LOAD_AT_PERIOD
						1	LOAD_IMMEDIATE
	1	FINTEN	RW	0x0	Counter stop after finite period or runs forever.	0	ENDLESS_RUN_MODE
						1	FINITE_PERIOD_MODE
	0	CNTRUN	RW	0x0	Counter run control. When this bit is enabled, counter starts to run and direction is up-counting.	0	DISABLE
						1	ENABLE
Reserved	0x0008	All		0x00000000	Control all the buffer/active structure timing		
	31:0	Reserved	RO	0x0			
ETSAWSYNC	0x000C	All	Protect	0x00000000	Saw-Wave Synchronization Control Register		
	31	Reserved	RO	0x0			
	30:28	OUT_DIV	RW	0x0	Synchronization output event divider	(x)	ADD_ONE_(x)
	27	Reserved	RO	0x0			
	26:24	OUT_SEL	RW	0x0	Synchronization output select	0	SYNCI
						1	SAWCNT_EQU_ZERO
						2	SAWCNT_EQU_CMP
						3	RESERVED
						4	RESERVED
						5	RESERVED
						6	RESERVED
						7	RESERVED
	23	Reserved	RO	0x0			
	22:20	IN_DIV	RW	0x0	Synchronization input event divider	(x)	ADD_ONE_(x)
	19	DLY_BYPASS	RW	0x0	Synchronization signal bypass delay block	0	NORMAL
						1	BYPASS
	18:16	IN_SEL	RW	0x0	Synchronization input select	0	MTPWM0_SYNC_OUT
						1	MTPWM1_SYNC_OUT

						2	ETIMER0_SYNC_OUT
						3	ETIMER1_SYNC_OUT
						4	ETIMER2_SYNC_OUT
						5	RESERVED
						6	RESERVED
						7	RESERVED
	15:4	Reserved	RO	0x0			
	3	SWTRIGOUT	W1S	0x0	Software trigger output synchronization pulse This event is ORed with SYNC input	0	NO_EFFECT
						1	ENABLE
	2	SWTRIGIN	W1S	0x0	Software trigger input synchronization pulse This event is ORed with SYNCI input	0	NO_EFFECT
						1	ENABLE
	1	OUT_EN	RW	0x0	Sync pulse output enable register	0	SAWCNT_SYNC_OUT_DISABLE
						1	SAWCNT_SYNC_OUT_ENABLE
	0	IN_EN	RW	0x0	Sync pulse input enable register	0	SAWCNT_SYNC_IN_DISABLE
						1	SAWCNT_SYNC_IN_ENABLE
CAPCTL	0x0010	All		0x00000000	Capture Control Register		
	31:28	Reserved	RO	0x0			
	27:24	SIG_SRC	RW	0x0	Capture Signal Source	0	EXTI_PIN
						1	INTERNAL_SIGNAL_0
						2	INTERNAL_SIGNAL_1
						3	RESERVED
						4	LIRC
						5	RESERVED
						6	ACMP_0_OUT
						7	ACMP_1_OUT
						8	ACMP_2_OUT
						9	ACMP_3_OUT
						10	RESERVED
						11	UART0_RX
						12	UART1_RX
						13	UART2_RX
						14	RESERVED
						15	RESERVED
	23:22	Reserved	RO	0x0			
	21:20	EVT_NUM	RO	0x0	Event number register. Indicate event number. When event occurs, this register will plus 1 and wrap after EVT_CNT=EVT_PRD. This bit field can write by software.	0	NOW_IS_EVENT_A
						1	NOW_IS_EVENT_B

						2	NOW_IS_EVENT_C
						3	NOW_IS_EVENT_D
	19:18	EVT_PRD	RW	0x0	Event period register. In one-shot mode： This is the number (between 0-3) of captures allowed to occur before the CAP (A-D) registers are frozen, i.e., capture sequence is stopped. Continuous mode: Wrap value for continuous mode. This is the number (between 0-3) of the capture register in which the circular buffer wraps around and starts again.	00	ON_CAPTURE_EVENT_A
						01	ON_CAPTURE_EVENT_B
						10	ON_CAPTURE_EVENT_C
						11	ON_CAPTURE_EVENT_D
	17	MODE	RW	0x0	Continuous or one-shot mode control (applicable only in capture mode)	0	CONTINOUS_MODE
						1	ONESHOT_MODE
	16	START	W1S	0x0	Start to event capture state machine control. Note: This function is valid in one shot or continuous mode. In capture one-shot mode, this bit is auto return 0 when EVT_CNT=EVT_PRD. In continuous mode, this bit will not auto return 0.	0	DISABLE
						1	ENABLE
	15:14	Reserved	RO	0x0			
	13:9	EVT_DIV	RW	0x0	Input divider prescale select. For example, when event A configured as rising edge and ETDIV=2. That means real event A will occur after 4 rising edge. This feature is useful when frequency of input signal is very high such as we want to measure the LIRC or LXT signal width.	(x)	(x)
	8	EVTD_RST	RW	0x0	Capture Event D Reset ETCNT	0	NO_RESET_ON_CAPTURE
						1	RESET_ON_CAPTURE
	7	EVTC_RST	RW	0x0	Capture Event C Reset ETCNT	0	NO_RESET_ON_CAPTURE
						1	RESET_ON_CAPTURE
	6	EVTB_RST	RW	0x0	Capture Event B Reset ETCNT	0	NO_RESET_ON_CAPTURE

						1	RESET_ON_CAPTURE
	5	EVTA_RST	RW	0x0	Capture Event A Reset ETCNT	0	NO_RESET_ON_CAPTURE
						1	RESET_ON_CAPTURE
	4	EVTD_TYPE	RW	0x0	Capture Event D Type Select	0	TRIG_ON_RISING_EDGE
						1	TRIG_ON_FALLING_EDGE
	3	EVTC_TYPE	RW	0x0	Capture Event C Type Select	0	TRIG_ON_RISING_EDGE
						1	TRIG_ON_FALLING_EDGE
	2	EVTB_TYPE	RW	0x0	Capture Event B Type Select	0	TRIG_ON_RISING_EDGE
						1	TRIG_ON_FALLING_EDGE
	1	EVTA_TYPE	RW	0x0	Capture Event A Type Select	0	TRIG_ON_RISING_EDGE
						1	TRIG_ON_FALLING_EDGE
	0	LOADEN	RW	0x0	Enable Loading of CAP A-D registers on a capture event	0	CAPTURE_LOAD_DISABLE
						1	CAPTURE_LOAD_ENABLE
Reserved	0x0014	All	RO				
	31:0	Reserved	RO	0x0			
ETCNT	0x0020	All		0x00000000	Enhenced Time Counter Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0	Active 16-bit counter register that is used as the capture time-base. This value can be updated by firmware cross software sync function.	(x)	(x)
ETSYNCRLD	0x0024	All		0x00000000	Counter reload value when sync in event occurs		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0	Counter phase value register that can be programmed for phase lag/lead	(x)	(x)
Reserved	0x0028	All	RO				
	31:0	Reserved	RO	0x0			
REGA_PRD_ACT	0x0030	All		0x00000000	Register A for capture and period(Active) register for PWM		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0	This register can be loaded by: - Time-Stamp(i.e., counter value) during a capture event - PRD shadow register(i.e., CAP2) when used in PWM mode	(x)	(x)
REGB_CMP_ACT	0x0034	All		0x00000000	Register B for capture and comparator(Active) register for PWM		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0	This register can be loaded by: - Time-Stamp(i.e., counter value) during a capture event - Software - may be useful for test purposes or initialization - APRD shadow register(i.e., CAP3) when used in PWM mode	(x)	(x)
REGC_PRD	0x0038	All		0x00000000	Register C for capture and period register for PWM		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0	In Capture mode, this is a time-stamp capture register. In PWM mode, this is the period register. You update the PWM period value through this register. In this mode, CAP0 is active register of CAP2_PRD_ACT.	(x)	(x)
REGD_CMP	0x003C	All		0x00000000	Register D for capture and		

					comparator register for PWM		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0	In Capture mode, this is a time-stamp capture register. In PWM mode, this is the compare shadow (ACMP) register. You update the PWM compare value via this register. In this mode, CAP3 (ACMP) shadows CAP1.	(x)	(x)
Reserved	0x0040	All	RO				
	31:0	Reserved	RO	0x0			
ETINT	0x0050	All		0x00000000	ETIMER Interrupt Control Register		
	31:17	Reserved	RO	0x0			
	16	BRAKE	RW	0x0	Brake event interrupt enable	0	DISABLE
						1	ENABLE
	15	PRD_OVF	RW	0x0	Counter Period Overflow Interrupt Enable This bit is set when a new timer period event occurs and the old one flag is not cleared.	0	DISABLE
						1	ENABLE
	14:10	Reserved	RO	0x0			
	9	CMP_UP	RW	0x0	This interrupt occurs when ETCNT=CMP at up counting This flag is active only in PWM (Timer) mode.	0	DISABLE
						1	ENABLE
	8	PRD	RW	0x0	E Period Interrupt Enable	0	DISABLE
						1	ENABLE
	7:4	Reserved	RO	0x0			
	3	EVT_CAPD	RW	0x0	Capture Event 3 Interrupt Enable	0	DISABLE
						1	ENABLE
	2	EVT_CAPC	RW	0x0	Capture Event 2 Interrupt Enable	0	DISABLE
						1	ENABLE
	1	EVT_CAPB	RW	0x0	Capture Event 1 Interrupt Enable	0	DISABLE
						1	ENABLE
	0	EVT_CAPA	RW	0x0	Capture Event 0 Interrupt Enable	0	DISABLE
						1	ENABLE
ETFLG	0x0054	All		0x00000000	ETIMER Event Flag(latched) Register		
	31:17	Reserved	RO	0x0			
	16	BRAKE	W1C	0x0	Brake event flag. When this bit is set, the PWM waveform stop to output. Only when this bit is clear, PWM returns normal.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	15	PRD_OVF	W1C	0x0	Counter Overflow Status Flag. This flag is active in Capture and PWM (Timer) mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	14:10	Reserved	RO	0x0			
	9	CMP_UP	W1C	0x0	This flag is set when ETCNT=CMP at up counting This flag is active only in PWM (Timer) mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	PRD	W1C	0x0	Counter Equal Period Status Flag This flag is only active in PWM (Timer) mode.	0	NOT_OCCUR

						1	OCCUR\WRITE_1_CLEAR
	7:4	Reserved	RO	0x0			
	3	EVT_CAPD	W1C	0x0	Capture Event D Status Flag This flag is only active in Capture mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	EVT_CAPC	W1C	0x0	Capture Event C Status Flag This flag is active only in Capture mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	EVT_CAPB	W1C	0x0	Capture Event B Status Flag This flag is only active in Capture mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	EVT_CAPA	W1C	0x0	Capture Event A Status Flag This flag is only active in Capture mode.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
ETINT_SWTRIG	0x0058	All		0x00000000	Enhenced timer software trigger interrupt register		
	31:17	Reserved	RO	0x0			
	16	BRAKE	W1S	0x0	Software trig brake event	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	15	PRD_OVF	W1S	0x0	Software trig Counter Overflow	0	NO_EFFECT
						1	FORCE_CNT_OVERFLOW
	14:10	Reserved	RO	0x0			
	9	CMP_UP	W1S	0x0	Software trig counter equal compare interrupt when up counting Interrupt	0	NO_EFFECT
						1	FORCE_CNT_EQU_COMP
	8	PRD	W1S	0x0	Software trig counter equal period interrupt when up counting Interrupt	0	NO_EFFECT
						1	FORCE_CNT_EQU_PRD
	7:4	Reserved	RO	0x0			
	3	EVT_CAPD	W1S	0x0	Software trig Capture Event 3	0	NO_EFFECT
						1	FORCE
	2	EVT_CAPC	W1S	0x0	Software trig Capture Event 2	0	NO_EFFECT
						1	FORCE
	1	EVT_CAPB	W1S	0x0	Software trig Capture Event 1	0	NO_EFFECT
						1	FORCE
	0	EVT_CAPA	W1S	0x0	Software trig Capture Event 0	0	NO_EFFECT
						1	FORCE

7.7 Cyclic Redundancy Check (CRC)

7.7.1 CRC Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
CRC_CTL	0x0000	ALL		0x00000000	CRC Control Register		
	31:8	Reserved	RO	0x0			
	7:6	POLYMODE	RW	0x0	CRC Polynomial Mode This field indicates the CRC operation polynomial mode.	0	CRC_16_CCITT_MODE
						1	CRC_8_MODE
						2	CRC_16_MODE

						3	CRC_32_MODE
	5	Reserved	RO	0x0			
	4	CRCFMT	RW	0x0	CRC Output Result Bit Order Reverse	0	DISABLE
						1	ENABLE
	3	DATFMT	RW	0x0	CRC Input Data Bit Order Reverse	0	DISABLE
						1	ENABLE
	2	CRC_BUSY	RO	0x0	CRC Busy	0	NO_EFFECT
						1	IS_BUSY
	1	CRC_RST	RW	0x0	CRC Engine Reset Note1: This bit will be cleared automatically. Note2: Setting this bit will reload the seed value from CRC_SEED register as checksum initial vale.	0	NO_EFFECT
						1	RESET_STATE_MACHINE
	0	CRC_EN	W1S	0x0	Enable CRC calculation by control register set.	0	NO_EFFECT
						1	WRITE_1_SET_ENABLE
CRC_SEED	0x0004	ALL		0x00000000	CRC Seed Register		
	31:0	CFC_SEED	RW	0x0	CRC Seed Value	(x)	
CRC_ADDR	0x0008	ALL		0x00000000	CRC Address Register		
	31:0	CRC_ADDR	RW	0x0	CRC Address Bits	(x)	
CRC_SIZE	0x000C	ALL		0x00000000	CRC Length Register		
	31:0	CRC_SIZE	RW	0x0	CRC Length Bits	(x)	
CRC_RESULT	0x0008	ALL		0x00000000	CRC Checksum Register		
	31:0	CRC_RESULT	RO	0x0	CRC Checksum Results	(x)	

7.8 Watchdog Timer (WDT)

7.8.1 WDT Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
WDOGLOAD	0x0000	ALL		0xFFFFFFFF	Watchdog Load Register		
	31:0	VAL	RW	0xFFFFFFFF	The WDOGLOAD Register is a 32 bits register containing the value from which the counter is to decrement. When this register is written to, the count is immediately restarted from the new value. The minimum valid value for WDOGLOAD is 1.		
WDOGVALUE	0x0004	ALL		0xFFFFFFFF	Watchdog Load Register		
	31:0	VAL	RO	0xFFFFFFFF	The WDOGVALUE Register gives the current value of the decrementing counter.		
WDOGCONTROL	0x0008	ALL		0x00000000	WDT Control Register		
	31:2	Reserved	RO	0x0			
	1	RESEN	RW	0X0	Enable watchdog reset output	0	DISABLE
						1	ENABLE
	0	INTEN	RW	0X0	Enable the interrupt event	0	DISABLE
						1	ENABLE
WDOGINTCLR	0x000C	ALL		0x00000000	Watchdog Clear Interrupt Register		
	31:1	Reserved	RO	0x0			
	0	CLR	W1C	0x0	A write of 1 to the WDOGINTCLR Register clears the watchdog interrupt, and reloads the counter from the value in WDOGLOAD.	0	NOT_OCCUR
						1	WRITE_1_CLEAR
WDOGRIS	0x0010	ALL		0x00000000	Watchdog Raw Interrupt Status Register		
	31:1	Reserved	RO	0x0			

	0	RESEN	RO	0X0	It indicates the raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt	0	NOT_OCCUR
						1	OCCUR
WDOGMIS	0x0014	ALL		0x00000000	Watchdog Interrupt Status Register		
	31:1	Reserved	RO	0x0			
	0	RESEN	RO	0X0	It indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the **INTEN** bit from the control register	0	NOT_OCCUR
						1	OCCUR

7.9 Real-Time Clock (RTC)

7.9.1 RTC Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	Label
RDATA	0x0000	All		0x00000000	RTC data register		
	31:0	VAL	RO	0x0	32-bit read data register. Reads from this register return the current value of the RTC	(x)	(x)
RMATCH	0x0004	All		0x00000000	RTC match register		
	31:0	DAT	RW	0x0	Writes to this register load the match register, and reads return the last written value. An equivalent match value is derived from this register. The derived value is compared with the counter value in the CLK1HZ domain to generate an interrupt	(x)	(x)
RLOAD	0x0008	All		0x00000000	RTC load register		
	31:0	DATA	RW	0x0	Writes to this register load an update value into the RTC Update logic block where the updated value of the RTC is calculated. Reads return the last written value.	(x)	(x)
RCTL	0x000C	All		0x00000000	RTC control register		
	31:1	Reserved	RO	0x0			
	0	start	W1C	0x0	If set to 1, the RTC is enabled. After the RTC is enabled, do not write to this bit otherwise the current RTC value is reset to zero	(x)	(x)
RINTMSK	0x0010	All		0x00000000	RTC Interrupt Mask Set or Clear register		
	31:1	Reserved	RO	0x0			
	0	IT_MASK_EN	RW	0x0	Controls the interrupt that the RTC generates	0	DISABLE_INTERRUPT
						1	ENABLE_INTERRUPT
RRAWINTSTS	0x0014	All	RO	0x00000000	RTC Raw Interrupt Status register		
	31:1	Reserved	RO	0x0			
	0	RIS	RO	0x0	Reading this register gives the current raw status value of the corresponding interrupt, prior to masking	(x)	(x)

RMSKINTSTS	0x0018	ALL	RW	0x00000000	RTC Masked Interrupt Status		
	31:1	Reserved	RO	0x0			
	0	MIS	RO	0x0	Reading this register gives the current masked status value of the corresponding interrupt.	(x)	(x)
RINTCLR	0x001C	All		0x00000000	RTC Interrupt Clear Register		
	31:1	Reserved	RO	0x0			
	0	ICR	W1C	0x0	Controls the masking of the interrupt that the RTC generates	0	NO_EFFECT
						1	CLEAR_INTERRUPT

7.10 Motor Pulse-Width Modulation (MTPWM)

FP5600 built-in 2 MTPWM units, designed for motor drive control applications. The MTPWM unit, as Figure 7-5, supports 6 PWM generators, configurable as 6 independent PWM outputs, or three complementary PWM pairs, as Figure 7-6, which are (MTPWMx_0A, MTPWMx_0B), (MTPWMx_1A, MTPWMx_1B) and (MTPWMx_2A, MTPWMx_2B) with programmable Brake-Zone, Dead-Time module.

Each MTPWM output shares a 16-bit counter for PWM period control and a 16-bit comparator for PWM duty cycle control. The MTPWM generator provides one general PWM interrupt which are set by hardware when the PWM period counter comparison matches the period and duty cycle, and one interrupt for Brake-Zone to prevent motor overcurrent.

The MTPWM Brake-Zone module can be configured as One-Shot mode, which generates only one PWM braking signal, or as Cycle-by-Cycle mode, which continuously performs PWM braking.

In addition to PWM, motor control requires analog comparator (ACOMP) and Analog-to-Digital Converter (ADC) to work together. In order to control and protect the motor more precisely, as Figure 7-7, some modules are provided, which can configure not only ADC Trigger, but also ACOMP overcurrent protection.

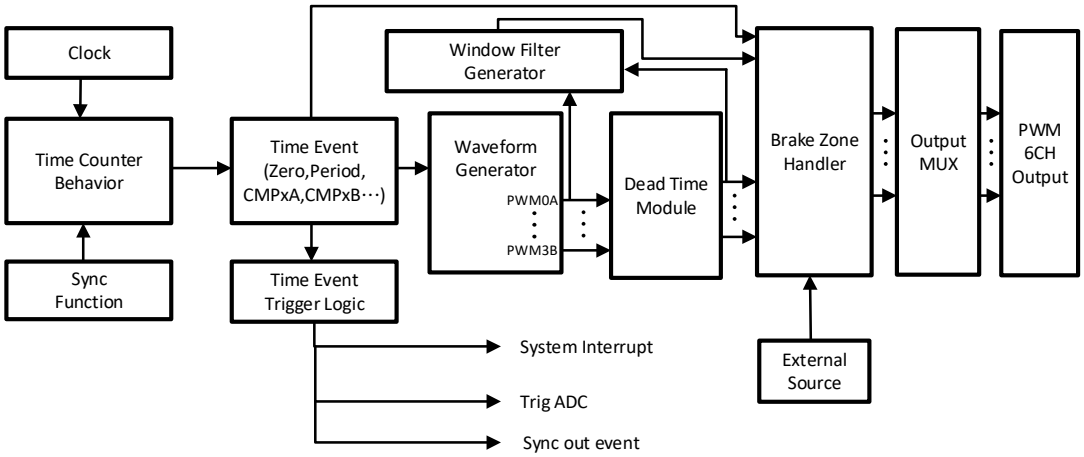


Figure 7-5 MTPWM Block Diagram

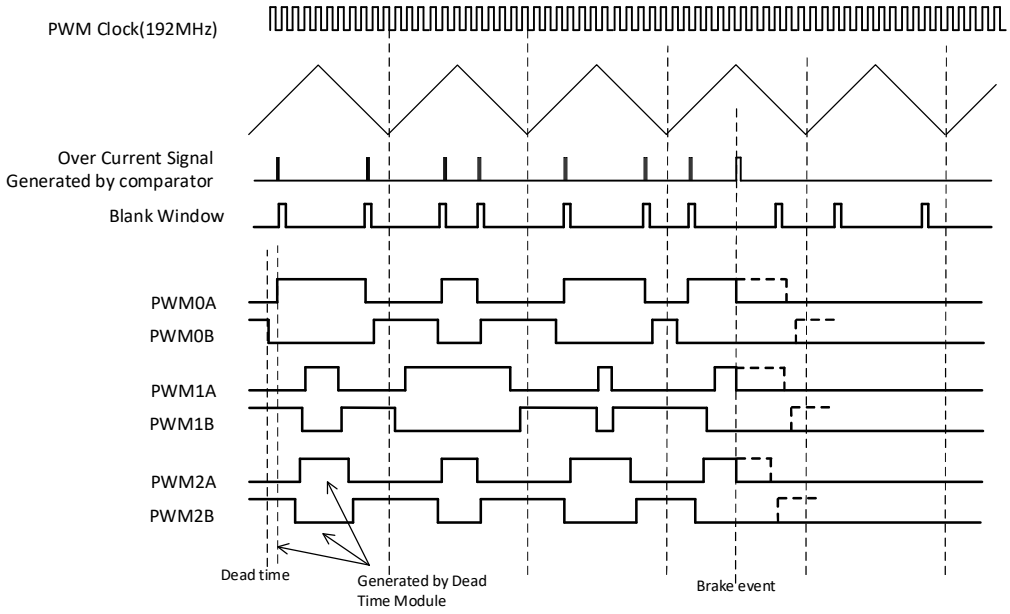


Figure 7-6 MTPWM signal example

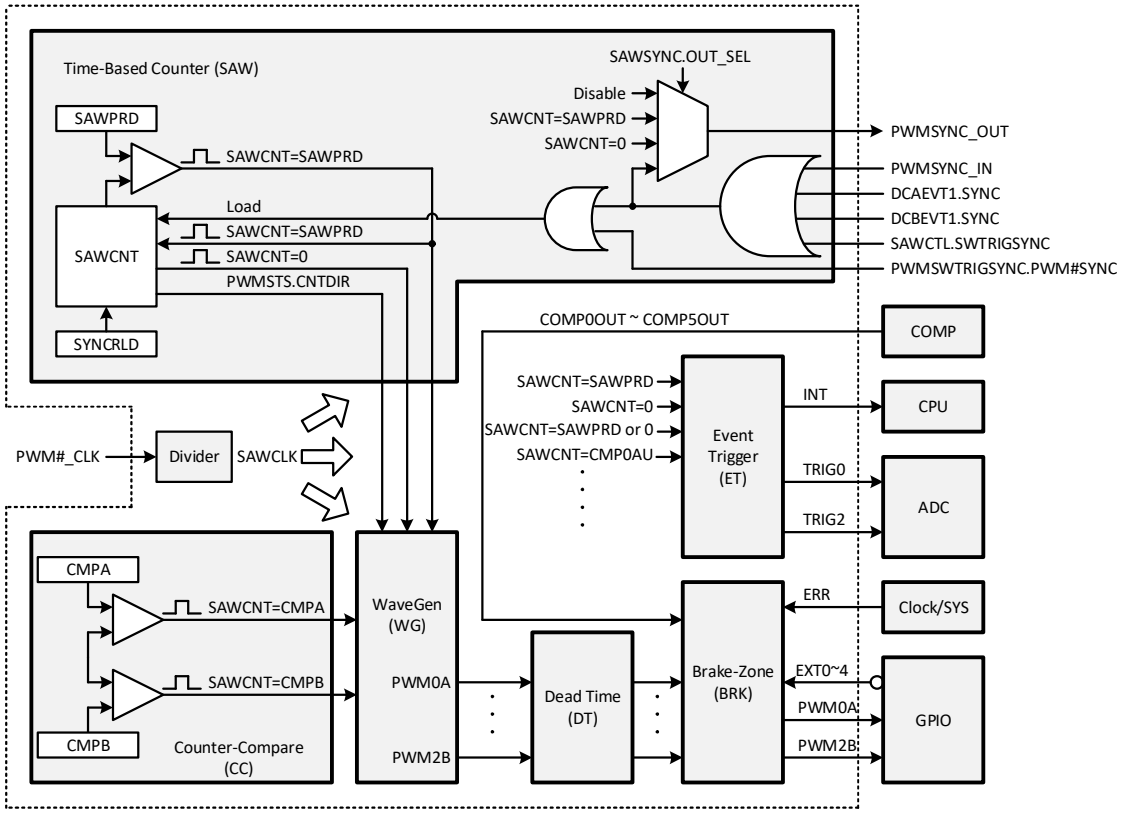


Figure 7-7 MTPWM with other modules

7.10.1 MTPWM Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
SAWCTL	0x0000	All	Protect	0x00000000	Saw-Wave Control Register		
	31	Reserved	RO	0x0			

	30:24	SAWCLKDIV	RW	0x0	Saw-Wave clock dividing ratio from PWM clock input	(x)	ADD_ONE_(x)
	23:15	Reserved	RO	0x0			
	14:13	DBGSTOP	RW	0x0	Software emulation mode It define the SAWCNT behavior when CPU hault in debug mode.	0	STOP_AFTER_PERIOD
						1	STOP_AFTER_CLOCK
						2	KEEP_RUN
						3	Reserved
	12:8	FINTNUM	RW	0x0	PWM number(a full period) counter when finite mode(5 bit)	(x)	(x)
	7:4	Reserved	RO	0x0			
	3:2	CNTTYPE	RW	0x0	Counter Type	0	COUNT_UP
						1	COUNT_DOWN
						2	COUNT_UP_DOWN
						3	Reserved
	1	FINTEN	RW	0x0	Counter stop after finite period or runs forever.	0	ENDLESS_RUN_MODE
						1	FINITE_PERIOD_MODE
	0	CNTRUN	RW	0x0	Counter run control	0	DISABLE
						1	ENABLE
LOADCTL	0x0004	All		0x00000000	Control all the buffer/active structure timing		
	31:10	Reserved	RO	0x0			
	9:8	TIMING	RW	0x0	Configure the double buffer register update timing	0	ON_ZERO_RELOAD
						1	ON_PERIOD_RELOAD
						2	ON_ZERO_OR_PERIOD_RELOAD
						3	FREEZE
	7:1	Reserved	RO	0x0			
	0	TYPE	RW	0x0	Saw-Wave counter period register (SAWPRD) load type	0	LOAD_AT_CONFIG_TIMING
						1	LOAD_IMMEDIATE
Reserved	0x0008	All	RO				
	31:0	Reserved	RO	0x0			
SAWSYNC	0x0010	All	Protect	0x00000000	Saw-Wave Synchronization Control Register		
	31	Reserved	RO	0x0			
	30:28	OUT_DIV	RW	0x0	Synchronization output event divider	(x)	ADD_ONE_(x)
	27	Reserved	RO	0x0			
	26:24	OUT_SEL	RW	0x0	Synchronization output select	0	SYNCI
						1	SAWCNT_EQU_ZERO
						2	SAWCNT_EQU_PREIOD
						3	SAWCNT_EQU_CMPTRIG1_UP_COUNT

						4	SAWCNT_EQU_CMPTRIG1_DOWN_COUNT
						5	SAWCNT_EQU_CMPTRIG2_UP_COUNT
						6	SAWCNT_EQU_CMPTRIG2_DOWN_COUNT
						7	Reserved
	23	Reserved	RO	0x0			
	22:20	IN_DIV	RW	0x0	Synchronization input event divider	(x)	ADD_ONE_(x)
	19	DLY_BYPASS	RW	0x0	Synchronization signal bypass delay block	0	NORMAL
						1	BYPASS
	18:16	IN_SEL	RW	0x0	Synchronization input select	0	MTPWM0_SYNC_OUT
						1	MTPWM1_SYNC_OUT
						2	ETIMER0_SYNC_OUT
						3	ETIMER1_SYNC_OUT
						4	ETIMER2_SYNC_OUT
						5	Reserved
						6	Reserved
						7	Reserved
	15:4	Reserved	RO	0x0			
	3	SWTRIGOUT	W1S	0x0	Software trigger output synchronization pulse This event is ORed with SYNC input	0	NO_EFFECT
						1	ENABLE
	2	SWTRIGIN	W1S	0x0	Software trigger input synchronization pulse This event is ORed with SYNCI input	0	NO_EFFECT
						1	ENABLE
	1	OUT_EN	RW	0x0	Sync pulse output enable register	0	SAWCNT_SYNC_OUT_DISABLE
						1	SAWCNT_SYNC_OUT_ENABLE
	0	IN_EN	RW	0x0	Sync pulse input enable register	0	SAWCNT_SYNC_IN_DISABLE
						1	SAWCNT_SYNC_IN_ENABLE
SYNCRLD	0x0014	All		0x00000000	Saw-Wave Counter Sync Reload Register		
	31:16	Reserved	RO	0x0			
	16	CNTDIR	RW	0x0	Counter direction after sync event It is valid only when SAWCNT is in up-down-count mode.	0	COUNT_DOWN_AFTER_SYNC
						1	COUNT_UP_AFTER_SYNC
	15:0	VAL	RW	0x0	Saw-Wave counter phase when synchronization event occurs	(x)	(x)
Reserved	0x0018	All	RO				
	31:0	Reserved	RO	0x0			
SAWPRD	0x0020	ALL	Protect	0x00000000	Saw-Wave Period Register(Buffer)		
	31:16	Reserved	RO	0x0			

	15:0	VAL	RW	0x0	Saw-Wave counter period	(x)	(x)
SAWPRDACT	0x0024	ALL		0x00000000	Saw-Wave Period Register Active		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0	Active Saw-Wave counter period	(x)	(x)
Reserved	0x0028	All	RO				
	31:0	Reserved	RO	0x0			
CMP0A	0x0030	All		0x00000000	Counter-Compare 0A Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMP0B	0x0034	All		0x00000000	Counter-Compare 0B Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMP1A	0x0038	All		0x00000000	Counter-Compare A Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMP1B	0x003C	All		0x00000000	Counter-Compare A Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			

	15:0	VAL	RW	0x0		(x)	(x)
CMP2A	0x0040	All		0x00000000	Counter-Compare A Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMP2B	0x0044	All		0x00000000	Counter-Compare 2B Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMPTRIG0	0x0048	All		0x00000000	Counter-Compare Trigger 0 Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMPTRIG1	0x004C	All		0x00000000	Counter-Compare Trigger 1 Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RW	0x0		(x)	(x)
CMPTRIG2	0x0050	All		0x00000000	Counter-Compare Trigger 2 Threshold Register(Buffer)		
	31:16	Reserved	RO	0x0			

	15:0	VAL	RW	0x0		(x)	(x)
CMP0AACT	0x0054	All		0x00000000	Counter-Compare 0A Threshold Active Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMP0BACT	0x0058	All		0x00000000	Counter-Compare 0B Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMP1AACT	0x005C	All		0x00000000	Counter-Compare 1A Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMP1BACT	0x0060	All		0x00000000	Counter-Compare 1B Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMP2AACT	0x0064	All		0x00000000	Counter-Compare 2A Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMP2BACT	0x0068	All		0x00000000	Counter-Compare 2B Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMPTRIG0ACT	0x006C	All		0x00000000	Counter-Compare Trigger 0 Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMPTRIG1ACT	0x0070	All		0x00000000	Counter-Compare Trigger 1 Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
CMPTRIG2ACT	0x0074	All		0x00000000	Counter-Compare Trigger 2 Threshold Register		
	31:16	Reserved	RO	0x0			
	15:0	VAL	RO	0x0		(x)	(x)
Reserved	0x0078	All	RO				
	31:0	Reserved	RO	0x0			
WAVGEN0A	0x0090	All		0x00000000	Generate Source Waveform of PWM0A channel		
	31:12	Reserved	RO	0x0			
	11:10	C0BD	RW	0x0	Action on output 0A when SAWCNT=CMP0B and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C0BU	RW	0x0	Action on output 0A when SAWCNT=CMP0B and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH

						3	RESERVED
	7:6	C0AD	RW	0x0	Action on output 0A when SAWCNT=CMP0A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C0AU	RW	0x0	Action on output 0A when SAWCNT=CMP0A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 0A when SAWCNT=SAWPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 0A when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
WAVGEN0B	0x0094	All		0x00000000	Generate Source Waveform of PWM0B channel		
	31:12	Reserved	RO	0x0			
	11:10	C0BD	RW	0x0	Action on output 0B when SAWCNT=CMP0B and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C0BU	RW	0x0	Action on output 0B when SAWCNT=CMP0B and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	7:6	C0AD	RW	0x0	Action on output 0B when SAWCNT=CMP0A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C0AU	RW	0x0	Action on output 0B when SAWCNT=CMP0A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 0B when SAWCNT=T0BPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 0B when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED

WAVGEN1A	0x0098	All		0x00000000	Generate Source Waveform of PWM1A channel		
	31:12	Reserved	RO	0x0			
	11:10	C1BD	RW	0x0	Action on output 1A when SAWCNT=CMP1B and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C1BU	RW	0x0	Action on output 1A when SAWCNT=CMP1B and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	7:6	C1AD	RW	0x0	Action on output 1A when SAWCNT=CMP1A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C1AU	RW	0x0	Action on output 1A when SAWCNT=CMP1A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 1A when SAWCNT=SAWPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 1A when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
WAVGEN1B	0x009C	All		0x00000000	Generate Source Waveform of PWM1B channel		
	31:12	Reserved	RO	0x0			
	11:10	C1BD	RW	0x0	Action on output 1B when SAWCNT=CMP1B and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C1BU	RW	0x0	Action on output 1B when SAWCNT=CMP1B and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	7:6	C1AD	RW	0x0	Action on output 1B when SAWCNT=CMP1A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C1AU	RW	0x0	Action on output 1B when SAWCNT=CMP1A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW

						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 1B when SAWCNT=SAWPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 1B when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
WAVGEN2A	0x00A0	All		0x00000000	Generate Source Waveform of PWM2A channel		
	31:12	Reserved	RO	0x0			
	11:10	C2BD	RW	0x0	Action on output 2A when SAWCNT=CMP2B and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C2BU	RW	0x0	Action on output 2A when SAWCNT=CMP2B and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	7:6	C2AD	RW	0x0	Action on output 2A when SAWCNT=CMP2A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C2AU	RW	0x0	Action on output 2A when SAWCNT=CMP2A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 2A when SAWCNT=SAWPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 2A when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
WAVGEN2B	0x00A4	All		0x00000000	Generate Source Waveform of PWM2B channel		
	31:12	Reserved	RO	0x0			
	11:10	C2BD	RW	0x0	Action on output 2B when SAWCNT=CMP2B nd SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	9:8	C2BU	RW	0x0	Action on output 2B when SAWCNT=CMP2B and SAWCNT is counting up	0	DO_NOTHING

						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	7:6	C2AD	RW	0x0	Action on output 2B when SAWCNT=CMP2A and SAWCNT is counting down	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	5:4	C2AU	RW	0x0	Action on output 2B when SAWCNT=CMP2A and SAWCNT is counting up	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	3:2	PRD	RW	0x0	Action on output 2B when SAWCNT=SAWPRD	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
	1:0	ZRO	RW	0x0	Action on output 2B when SAWCNT=Zero	0	DO_NOTHING
						1	SET_LOW
						2	SET_HIGH
						3	RESERVED
Reserved	0x00A8	All	RO				
	31:0	Reserved	RO	0x0			
GENMUX	0x00B0	All	Protect	0x00000000	PWM waveform pin out mux		
	31:25	Reserved	RO	0x0			
	24	BUFMODE	RW	0x0	Load mode control.	0	LOAD_AT_CONFIG_TIMING
						1	LOAD_IMMEDIATE
	23:22	Reserved	RO	0x0			
	21	MUX2B	RW		PWM2B final waveform selection. The waveform can directly controlled by configured level as DAT2B.	0	AS_DATA
						1	AS_PWM_GEN
	20	MUX2A	RW		PWM2A final waveform selection. The waveform can directly controlled by configured level as DAT2A.	0	AS_DATA
						1	AS_PWM_GEN
	19	MUX1B	RW		PWM1B final waveform selection. The waveform can directly controlled by configured level as DAT1B.	0	AS_DATA
						1	AS_PWM_GEN
	18	MUX1A	RW		PWM1A final waveform selection. The waveform can directly controlled by configured level as DAT1A.	0	AS_DATA
						1	AS_PWM_GEN

	17	MUX0B	RW		PWM0B final waveform selection. The waveform can directly controlled by configured level as DAT0B.	0	AS_DATA
						1	AS_PWM_GEN
	16	MUX0A	RW		PWM0A final waveform selection. The waveform can directly controlled by configured level as DAT0A.	0	AS_DATA
						1	AS_PWM_GEN
	15:6	Reserved	RO	0x0			
	5	DAT2B	RW	0x0	Continuous software force on output 2B The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
	4	DAT2A	RW	0x0	Continuous software force on output 2A The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
	3	DAT1B	RW	0x0	Continuous software force on output 1B The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
	2	DAT1A	RW	0x0	Continuous software force on output 1A The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
	1	DAT0B	RW	0x0	Continuous software force on output 0B The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
	0	DAT0A	RW	0x0	Continuous software force on output 0A The register can be in immediate mode or double buffer mode as determined by GENMUX.BUFMODE.	0	SET_LOW
						1	SET_HIGH
Reserved	0x00B4	All	RO				
	31:0	Reserved	RO	0x0			
DTCTL	0x00C0	All	Protect	0x00000000	Dead-Time Generator Control Register		
	31	DTCLKDIV	RW	0x0	Clock divider for RDTDLY and FDTDLY. DIV=DTCLKDIV+1	0	DIV_1
						1	DIV_2
	30:22	Reserved	RO	0x0			
	21	OUT2B	RW	0x0	PWM2B output source selection	0	FROM_ORIGNAL_GEN_2B

						1	FROM_DEAD_TIME_CH_2B
	20	OUT2A	RW	0x0	PWM2A output source selection	0	FROM_ORIGNAL_GEN_2A
						1	FROM_DEAD_TIME_CH_2A
	19	INV2B	RW	0x0	PWM2B inverse source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	18	INV2A	RW	0x0	PWM2A inverse delay source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	17	FALLSRC2	RW	0x0	PWM2B Falling-edge delay source selection	0	FROM_GEN_2A
						1	FROM_GEN_2B
	16	RISESRC2	RW	0x0	PWM2A Rising-edge delay source selection	0	FROM_GEN_2A
						1	FROM_GEN_2B
	15:14	Reserved	RO	0x0			
	13	OUT1B	RW	0x0	PWM1B output source selection	0	FROM_ORIGNAL_GEN_1B
						1	FROM_DEAD_TIME_CH_1B
	12	OUT1A	RW	0x0	PWM1A output source selection	0	FROM_ORIGNAL_GEN_1A
						1	FROM_DEAD_TIME_CH_1A
	11	INV1B	RW	0x0	PWM1B inverse source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	10	INV1A	RW	0x0	PWM1A inverse delay source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	9	FALLSRC1	RW	0x0	PWM1B Falling-edge delay source selection	0	FROM_GEN_1A
						1	FROM_GEN_1B
	8	RISESRC1	RW	0x0	PWM1A Rising-edge delay source selection	0	FROM_GEN_1A
						1	FROM_GEN_1B
	7:6	Reserved	RO	0x0			
	5	OUT0B	RW	0x0	PWM0B output source selection	0	FROM_ORIGNAL_GEN_0B
						1	FROM_DEAD_TIME_CH_0B
	4	OUT0A	RW	0x0	PWM0A output source selection	0	FROM_ORIGNAL_GEN_0A
						1	FROM_DEAD_TIME_CH_0A
	3	INV0B	RW	0x0	PWM0B inverse source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	2	INV0A	RW	0x0	PWM0A inverse delay source selection	0	WITH_DELAY
						1	WITH_DELAY_AND_INVERTER
	1	FALLSRC0	RW	0x0	PWM0B Falling-edge delay source selection	0	FROM_GEN_0A
						1	FROM_GEN_0B
	0	RISESRC0	RW	0x0	PWM0A Rising-edge delay source selection	0	FROM_GEN_0A
						1	FROM_GEN_0B
RDTDLY	0x00C4	All	Protect	0x00000000	Rising Dead-time Delay Register		
	31:10	Reserved	RO	0x0			
	9:0	VAL	RW	0x0	Rising-edge delay	(x)	(x)
FDTDLY	0x00C8	All		0x00000000	Falling Dead-time Delay Register		
	31:10	Reserved	RO	0x0			

	9:0	VAL	RW	0x0	Falling-edge delay	(x)	(x)
Reserved	0x00CC	All	RO				
	31:0	Reserved	RO	0x0			
BRKCBCSEL	0x00D0	All	Protect	0x00000000	Brake-stop Select Register		
	31:6	Reserved	RO	0x0			
	5	SLFCHK	RW	0x0	Brake PWM signal when self check signal. This selection is reserved now.	0	DISABLE
						1	ENABLE
	4	DEBUGSTOP	RW	0x0	Brake PWM signal when stop signal in debug mode.	0	DISABLE
						1	ENABLE
	3	SYSERR	RW	0x0	System error should be RAM parity check, clock error, BOD signal…	0	DISABLE
						1	ENABLE
	2	DICOMP	RW	0x0	Source from ADC digital comparator, select signals from BRKDICOMPSEL.	0	DISABLE
						1	ENABLE
	1	ACOMP	RW	0x0	Source from internal analog comparator, select signals from BRKCOMPSEL	0	DISABLE
						1	ENABLE
	0	EXTPIN	RW	0x0	Source from external pin, select signals and polarity(active high or low) from BRKEXTSEL	0	DISABLE
						1	ENABLE
BRKOSTSEL	0x00D4	All	Protect	0x00000000	Brake-stop Select Register		
	31:5	Reserved	RO	0x0			
	4	DEBUGSTOP	RW	0x0	Brake PWM signal when stop signal when debug mode.	0	DISABLE
						1	ENABLE
	3	SYSERR	RW	0x0	System error should be RAM parity check, clock error, BOD signal…	0	DISABLE
						1	ENABLE
	2	DICOMP	RW	0x0	Source from ADC digital comparator, select signals from BRKDICOMPSEL.	0	DISABLE
						1	ENABLE
	1	ACOMP	RW	0x0	Source from internal analog comparator, select signals from BRKCOMPSEL	0	DISABLE
						1	ENABLE
	0	EXTPIN	RW	0x0	Source from external pin, select signals and polarity(active high or low) from BRKEXTSEL	0	DISABLE
						1	ENABLE
BRKEXTSEL	0x00D8	All	Protect	0x00000000	Brake-stop Source External Pin Select Register		
	31:19	Reserved	RO	0x0			
	18	EXT2WFILT	RW	0x0	Determine the EXT2(After polarity set) signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	17	EXT1WFILT	RW	0x0	Determine the EXT1(After polarity set) signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	16	EXT0WFILT	RW	0x0	Determine the EXT0(After	0	DO_NOT_FILT

					polarity set) signal go through with window filter or not		
						1	WITH_WINDOW_FILT
	15:11	Reserved	RO	0x0			
	10	EXT2POL	RW	0x0	Select BRK2 polarity is active H or L.	0	ACTIVE_HIGH
						1	ACTIVE_LOW
	9	EXT1POL	RW	0x0	Select BRK1 polarity is active H or L.	0	ACTIVE_HIGH
						1	ACTIVE_LOW
	8	EXT0POL	RW	0x0	Select BRK0 polarity is active H or L.	0	ACTIVE_HIGH
						1	ACTIVE_LOW
	7:3	Reserved	RO	0x0			
	2	EXT2	RW	0x0	BRK2 is an external pin select form pin mux. Select BRK4 as the source of EXTPIN in BRKOSTSEL and BRKCBCSEL.	0	DISABLE
						1	ENABLE
	1	EXT1	RW	0x0	BRK1 is an external pin select form pin mux. Select BRK4 as the source of EXTPIN in BRKOSTSEL and BRKCBCSEL.	0	DISABLE
						1	ENABLE
	0	EXT0	RW	0x0	BRK0 is an external pin select form pin mux. Select BRK4 as the source of EXTPIN in BRKOSTSEL and BRKCBCSEL.	0	DISABLE
						1	ENABLE
BRKACOMPSEL	0x00DC	All	Protect	0x00000000	Brake-stop Source Analog Comparator Select Register		
	31:20	Reserved	RO	0x0			
	19	ACOMP3WFILT	RW	0x0	Determine the ACOMP3 signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	18	ACOMP2WFILT	RW	0x0	Determine the ACOMP2 signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	17	ACOMP1WFILT	RW	0x0	Determine the AACOMP1 signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	16	ACOMP0WFILT	RW	0x0	Determine the ACOMP0 signal go through with window filter or not	0	DO_NOT_FILT
						1	WITH_WINDOW_FILT
	15:4	Reserved	RO	0x0			
	3	ACOMP3	RW	0x0	Select ACOMP3(after filter selection) signal as source of ACOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	2	ACOMP2	RW	0x0	Select ACOMP2(after filter selection) signal as source of ACOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	1	ACOMP1	RW	0x0	Select ACOMP1(after filter selection) signal as source of ACOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	0	ACOMP0	RW	0x0	Select ACOMP0(after filter selection) signal as source of	0	DISABLE

					ACOMP brake-stop signal.		
						1	ENABLE
BRKDICOMPSEL	0x00E0	All		0x00000000	Brake-stop Source Digital Comparator Select Register		
	31:4	Reserved	RO	0x0			
	3	DICOMP3	RW	0x0	Select DICOMP3 signal as source of DICOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	2	DICOMP2	RW	0x0	Select DICOMP2 signal as source of DICOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	1	DICOMP1	RW	0x0	Select DICOMP1 signal as source of DICOMP brake-stop signal.	0	DISABLE
						1	ENABLE
	0	DICOMP0	RW	0x0	Select DICOMP0 signal as source of DICOMP brake-stop signal.	0	DISABLE
						1	ENABLE
BRKSYSERRSEL	0x00E4	All	Protect	0x00000000	Brake-stop System Error Select Register		
	31:4	Reserved	RO	0x0			
	3	WDT	RW	0x0	Watchdog overflow. When watchdog overflow, PWM output should be turned off immediately.	0	DISABLE
						1	ENABLE
	2	BOD	RW	0x0	Select brown out detection event as source of SYSERR brake-stop signal.	0	DISABLE
						1	ENABLE
	1	CLKFAIL	RW	0x0	Select clock fail signal such as PLL or HIRC fail as source of SYSERR brake-stop signal.	0	DISABLE
						1	ENABLE
	0	Reserved	RO	0x0			
BRKWAVCTL	0x00E8	All	Protect	0x00000000	Brake-stop Control Register		
	31:12	Reserved	RO	0x0			
	11:10	CH2B	RW	0x0	Action on output PWM 2B final output channel when a brake event occurs	0	TRI_STATE
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
	9:8	CH2A	RW	0x0	Action on output PWM 2A final output channel when a brake event occurs	0	TRI_STATE
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
	7:6	CH1B	RW	0x0	Action on output PWM 1B final output channel when a brake event occurs	0	TRI_STATE
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
	5:4	CH1A	RW	0x0	Action on output PWM 1A final output channel when a brake event occurs	0	TRI_STATE
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
	3:2	CH0B	RW	0x0	Action on output PWM 0B final	0	TRI_STATE

					output channel when a brake event occurs		
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
	1:0	CH0A	RW	0x0	Action on output PWM 0A final output channel when a brake event occurs	0	TRI_STATE
						1	SET_HIGH
						2	SET_LOW
						3	DO_NOTHING
BRKIE	0x00EC	All		0x00000000	Brake-stop Enable Interrupt Register		
	31:3	Reserved	RO	0x0			
	2	OST	RW	0x0	one-shot Brake-stop interrupt	0	DISABLE
						1	ENABLE
	1	CBC	RW	0x0	cycle-by-cycle Brake-stop interrupt	0	DISABLE
						1	ENABLE
	0	Reserved	RO	0x0			
BRKFLG0	0x00F0	All		0x00000000	Brake-stop Flag Register 0		
	31:13	Reserved	RO	0x0			
	13	SLFCHK	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	12	DEBUGSTOP	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	11	SYSERR	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	10	DICOMP	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	9	ACOMP	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	EXTPIN	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7:3	Reserved	RO	0x0			
	2	BRKINT	W1C	0x0	Latched brake interrupt status flag. Write 1 to clear this bit	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	OST	W1C	0x0	Latched one-shot brake event status flag. Write 1 to clear this bit.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	CBC	W1C	0x0	Latched cycle-by-cycle brake event status flag. Write 1 to clear this bit.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR

BRKFLG1	0x00F4	All		0x00000000	Brake-stop Flag Register 1		
	31:12	Reserved	RO	0x0			
	11	COMP3	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	10	COMP2	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	9	COMP1	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	COMP0	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7:3	Reserved	RO	0x0			
	2	EXT2	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	EXT1	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	EXT0	W1C	0x0	Event latched signal, only observe and write 1 clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
BRKFILTCTL	0x00F8	All	Protect	0x00000000	Generate brake-stop signal filter window The longest filter time in real world will not pass 10us		
	31:26	Reserved	RO	0x0			
	25	WPOL	RW	0x0	Window polarity	0	WITH_LOGIC_NOT
						1	GO_THROUGH
	24	SRC	RW	0x0	Window is selected from global window signal or local window generator.	0	FROM_LOCAL
						1	FROM_GLOBAL
	23	Reserved	RO	0x0			
	22	CH2BSRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME
						1	FROM_WAVE_GEN
	21	CH2BFEN	RW	0x0	Enable falling edge window on PWM 2B.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	20	CH2BREN	RW	0x0	Enable rising edge window on PWM 2B.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
	19	Reserved	RO	0x0			
	18	CH2ASRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME
						1	FROM_WAVE_GEN
	17	CH2AFEN	RW	0x0	Enable falling edge window on PWM 2A.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	16	CH2AREN	RW	0x0	Enable rising edge window on PWM 2A.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
	15	Reserved	RO	0x0			
	14	CH1BSRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME

						1	FROM_WAVE_GEN
	13	CH1BFEN	RW	0x0	Enable falling edge window on PWM 1B.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	12	CH1BREN	RW	0x0	Enable rising edge window on PWM 1B.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
	11	Reserved	RO	0x0			
	10	CH1ASRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME
						1	FROM_WAVE_GEN
	9	CH1AFEN	RW	0x0	Enable falling edge window on PWM 1A.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	8	CH1AREN	RW	0x0	Enable rising edge window on PWM 1A.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
	7	Reserved	RO	0x0			
	6	CH0BSRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME
						1	FROM_WAVE_GEN
	5	CH0BFEN	RW	0x0	Enable falling edge window on PWM 0B.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	4	CH0BREN	RW	0x0	Enable rising edge window on PWM 0B.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
	3	Reserved	RO	0x0			
	2	CH0ASRC	RW	0x0	Select edge detection source.	0	FROM_DEAD_TIME
						1	FROM_WAVE_GEN
	1	CH0AFEN	RW	0x0	Enable falling edge window on PWM 0A.	0	DISABLE_FALLING_EDGE
						1	ENABLE_FALLING_EDGE
	0	CH0AREN	RW	0x0	Enable rising edge window on PWM 0A.	0	DISABLE_RISING_EDGE
						1	ENABLE_RISING_EDGE
BRKFILTWIDTH	0x00FC	All	Protect	0x00000000	Generate brake-stop signal filter window The longest filter time in real world will not over than 10us		
	31:16	Reserved	RO	0x0			
	17:16	DIV	RW	0x0	divider, the filter window width is generated by clock after divider.	0	DIV_1
						1	DIV_2
						2	DIV_3
						3	DIV_4
	15:10	Reserved	RO	0x0			
	9:0	WIDTH	RW	0x0		(x)	(x)
Reserved	0x0100	All	RO				
	31:0	Reserved	RO	0x0			
Reserved	0x0104	All		0x00000000			
	31:0	Reserved	RO	0x0			
BRKSWTRIG	0x0108	All		0x00000000	Brake-stop Software Force Register		
	31:2	Reserved	RO	0x0			
	1	OST	W1S	0x0	Software Trigger a one-shot brake event	0	NO_EFFECT
						1	FORCE_OST_BRK

	0	CBC	W1S	0x0	Software Trigger a cycle-by-cycle brake event	0	NO_EFFECT
						1	FORCE_CBC_BRK
Reserved	0x010C	All	RO				
	31:0	Reserved	RO	0x0			
OUTEN	0x0110	All	Protect	0x00000000	PWM waveform pin out mux		
	31:6	Reserved	RO	0x0			
	5	CH2B	RW	0x0	Final channel output selection of PWM2B	0	AS_TRISTATE
						1	ENABLE
	4	CH2A	RW	0x0	Final channel output selection of PWM2A	0	AS_TRISTATE
						1	ENABLE
	3	CH1B	RW	0x0	Final channel output selection of PWM1B	0	AS_TRISTATE
						1	ENABLE
	2	CH1A	RW	0x0	Final channel output selection of PWM1A	0	AS_TRISTATE
						1	ENABLE
	1	CH0B	RW	0x0	Final channel output selection of PWM0B	0	AS_TRISTATE
						1	ENABLE
	0	CH0A	RW	0x0	Final channel output selection of PWM0A	0	AS_TRISTATE
						1	ENABLE
Reserved	0x010C	All	RO				
	31:0	Reserved	RO	0x0			
PWMSTS	0x0120	All		0x00000000	PWM Status(Non latched) Register		
	31	PWM2B_OUT	RO	0x0	Reflect PWM2B final output signal	0	LOW
						1	HIGH
	30	PWM2A_OUT	RO	0x0	Reflect PWM2A final output signal	0	LOW
						1	HIGH
	29	PWM1B_OUT	RO	0x0	Reflect PWM1B final output signal	0	LOW
						1	HIGH
	28	PWM1A_OUT	RO	0x0	Reflect PWM1A final output signal	0	LOW
						1	HIGH
	27	PWM0B_OUT	RO	0x0	Reflect PWM0B final output signal	0	LOW
						1	HIGH
	26	PWM0A_OUT	RO	0x0	Reflect PWM0A final output signal	0	LOW
						1	HIGH
	25	BRKOST	RO	0x0	Reflect BRKOST source signal(non-latched)	0	LOW
						1	HIGH
	24	BRKCBC	RO	0x0	Reflect BRKCBC source signal(non-latched)	0	LOW
						1	HIGH
	23:18	Reserved	RO	0x0			
	17	BRKFILT_OUT	RO	0x0	Reflect BRKFILT signal(non-latched)	0	LOW
						1	HIGH
	16	CNTDIR	RO	0x0	Saw-Wave counter direction status	0	COUNTING_DOWN
						1	COUNTING_UP
	15:0	**SAWCNT**	**RO**	0x0	Current value of the Saw-Wave	(x)	(x)

					counter		
SAWEVTFLG	0x0124	All		0x00000000	Saw-Wave Event Latched Flag Register		
	31	CNTMAX	W1C	0x0	Saw-Wave counter reaching max latched status	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	30	SYNC_OUT	W1C	0x0	Output synchronization latched status	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	29	SYNC_IN	W1C	0x0	Input synchronization latched status	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	28:21	Reserved	RO	0x0			
	20	CTRIG2D	W1C	0x0	COMPTRIG2 down counting event occur(latched)	0	CMPTRIG2_DOWN_COUNT_NOT_OCCUR
						1	CMPTRIG2_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	19	CTRIG2U	W1C	0x0	COMPTRIG2 Up counting event occur(latched)	0	CMPTRIG2_UP_COUNT_NOT_OCCUR
						1	CMPTRIG2_UP_COUNT_OCCUR \WRITE_1_CLEAR
	18	CTRIG1D	W1C	0x0	COMPTRIG1 down counting event occur(latched)	0	CMPTRIG1_DOWN_COUNT_NOT_OCCUR
						1	CMPTRIG1_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	17	CTRIG1U	W1C	0x0	COMPTRIG1 Up counting event occur(latched)	0	CMPTRIG1_UP_COUNT_NOT_OCCUR
						1	CMPTRIG1_UP_COUNT_OCCUR \WRITE_1_CLEAR
	16	CTRIG0D	W1C	0x0	COMPTRIG0 down counting event occur(latched)	0	CMPTRIG0_DOWN_COUNT_NOT_OCCUR
						1	CMPTRIG0_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	15	CTRIG0U	W1C	0x0	COMPTRIG0 Up counting event occur(latched)	0	CMPTRIG0_UP_COUNT_NOT_OCCUR
						1	CMPTRIG0_UP_COUNT_OCCUR \WRITE_1_CLEAR
	14	C2BD	W1C	0x0	COMP2A down counting event occur(latched)	0	CMP2B_DOWN_COUNT_NOT_OCCUR
						1	CMP2B_DOWN_COUNT_OCCUR
	13	C2BU	W1C	0x0	COMP2B Up counting event occur(latched)	0	CMP2B_UP_COUNT_NOT_OCCUR
						1	CMP2B_UP_COUNT_OCCUR \WRITE_1_CLEAR
	12	C2AD	W1C	0x0	COMP2A down counting event occur(latched)	0	CMP2A_DOWN_COUNT_NOT_OCCUR
						1	CMP2A_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	11	C2AU	W1C	0x0	COMP2A Up counting event occur(latched)	0	CMP2A_UP_COUNT_NOT_OCCUR
						1	CMP2A_UP_COUNT_OCCUR \WRITE_1_CLEAR

	10	C1BD	W1C	0x0	COMP1A down counting event occur(latched)	0	CMP1B_DOWN_COUNT_NOT_OCCUR
						1	CMP1B_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	9	C1BU	W1C	0x0	COMP1B Up counting event occur(latched)	0	CMP1B_UP_COUNT_NOT_OCCUR
						1	CMP1B_UP_COUNT_OCCUR \WRITE_1_CLEAR
	8	C1AD	W1C	0x0	COMP1A down counting event occur(latched)	0	CMP1A_DOWN_COUNT_NOT_OCCUR
						1	CMP1A_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	7	C1AU	W1C	0x0	COMP1A Up counting event occur(latched)	0	CMP1A_UP_COUNT_NOT_OCCUR
						1	CMP1A_UP_COUNT_OCCUR \WRITE_1_CLEAR
	6	C0BD	W1C	0x0	COMP0A down counting event occur(latched)	0	CMP0B_DOWN_COUNT_NOT_OCCUR
						1	CMP0B_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	5	C0BU	W1C	0x0	COMP0B Up counting event occur(latched)	0	CMP0B_UP_COUNT_NOT_OCCUR
						1	CMP0B_UP_COUNT_OCCUR \WRITE_1_CLEAR
	4	C0AD	W1C	0x0	COMP0A down counting event occur(latched)	0	CMP0A_DOWN_COUNT_NOT_OCCUR
						1	CMP0A_DOWN_COUNT_OCCUR \WRITE_1_CLEAR
	3	C0AU	W1C	0x0	COMP0A Up counting event occur(latched)	0	CMP0A_UP_COUNT_NOT_OCCUR
						1	CMP0A_UP_COUNT_OCCUR \WRITE_1_CLEAR
	2	Reserved	RO	0x0			
	1	PRD	W1C	0x0		0	PERIOD_OCCUR
						1	PERIOD_OCCUR \WRITE_1_CLEAR
	0	ZRO	W1C	0x0		0	ZERO_OCCUR
						1	ZERO_OCCUR \WRITE_1_CLEAR
INTCTL	0x0128	All		0x00000000	Select the interrupt source		
	31:29	EVTNUM	RW	0x0	PWM saw event interrupt(INT) number It indicates how many selected TRIG0 events have occurred. This field can be modified by firmware to adjust the phase of trigger sequence.	(x)	(x)
	28:27	Reserved	RO	0x0			
	26:24	EVTDIV	RW	0x0	PWM saw event interrupt(INT) divider select It determines how many selected TRIG0SEL events need to occur before a trigger pulse is generated.	(x)	ADD_ONE_(x)
	23:20	Reserved	RO	0x0			
	19	CMPTG2D	RW	0x0	PWM trigger interrupt when TRIG2 event at down counting	0	DISABLE

				enable		
					1	ENABLE
18	CMPTG2U	RW	0x0	PWM trigger interrupt when TRIG2 event at up counting enable	0	DISABLE
					1	ENABLE
17	CMPTG1D	RW	0x0	PWM trigger interrupt when TRIG1 event at down counting enable	0	DISABLE
					1	ENABLE
16	CMPTG1U	RW	0x0	PWM trigger interrupt when TRIG1 event at up counting enable	0	DISABLE
					1	ENABLE
15	CMPTG0D	RW	0x0	PWM trigger interrupt when TRIG0 event at down counting enable	0	DISABLE
					1	ENABLE
14	CMPTG0U	RW	0x0	PWM trigger interrupt when TRIG0 event at up counting enable	0	DISABLE
					1	ENABLE
13	CMP2BD	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2B at down counting	0	DISABLE
					1	ENABLE
12	CMP2BU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2B at up counting	0	DISABLE
					1	ENABLE
11	CMP2AD	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2A at down counting	0	DISABLE
					1	ENABLE
10	CMP2AU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2A at up counting	0	DISABLE
					1	ENABLE
9	CMP1BD	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2B at down counting	0	DISABLE
					1	ENABLE
8	CMP1BU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP2B at up counting	0	DISABLE
					1	ENABLE
7	CMP1AD	RW	0x0	PWM trigger interrupt when SAWCNT = CMP1A at down counting	0	DISABLE
					1	ENABLE
6	CMP1AU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP1A at up counting	0	DISABLE
					1	ENABLE
5	CMP0BD	RW	0x0	PWM trigger interrupt when SAWCNT = CMP0B at down counting	0	DISABLE
					1	ENABLE
4	CMP0BU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP0B at up counting	0	DISABLE
					1	ENABLE
3	CMP0AD	RW	0x0	PWM trigger interrupt when	0	DISABLE

					SAWCNT = CMP0A at down counting		
						1	ENABLE
	2	CMP0AU	RW	0x0	PWM trigger interrupt when SAWCNT = CMP0A at up counting	0	DISABLE
						1	ENABLE
	1	PERIOD	RW	0x0	PWM trigger interrupt when SAWCNT=Period	0	DISABLE
						1	ENABLE
	0	ZERO	RW	0x0	PWM trigger interrupt when SAWCNT=Zero	0	DISABLE
						1	ENABLE
TRIG0CTL	0x012C	All		0x00000000	TRIG0 signal Control Register		
	31:29	EVTNUM	RW	0x0	PWM trigger event 0(TRIG0) number It indicates how many selected TRIG0 events have occurred. This field can be modified by firmware to adjust the phase of trigger sequence.	(x)	(x)
	28:27	Reserved	RO	0x0			
	26:24	EVTDIV	RW	0x0	PWM trigger event 1(TRIG0) divider select It determines how many selected TRIG0 events need to occur before a trigger pulse is generated.	(x)	ADD_ONE_(x)
	23:20	Reserved	RO	0x0			
	19	CMPTG2D	RW	0x0	PWM trigger ADC signal when TRIG2 event at down counting enable	0	DISABLE
						1	ENABLE
	18	CMPTG2U	RW	0x0	PWM trigger ADC signal when TRIG2 event at up counting enable	0	DISABLE
						1	ENABLE
	17	CMPTG1D	RW	0x0	PWM trigger ADC signal when TRIG1 event at down counting enable	0	DISABLE
						1	ENABLE
	16	CMPTG1U	RW	0x0	PWM trigger ADC signal when TRIG1 event at up counting enable	0	DISABLE
						1	ENABLE
	15	CMPTG0D	RW	0x0	PWM trigger ADC signal when TRIG0 event at down counting enable	0	DISABLE
						1	ENABLE
	14	CMPTG0U	RW	0x0	PWM trigger ADC signal when TRIG0 event at up counting enable	0	DISABLE
						1	ENABLE
	13	CMP2BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
						1	ENABLE
	12	CMP2BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
						1	ENABLE
	11	CMP2AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at down counting	0	DISABLE

						1	ENABLE
	10	CMP2AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at up counting	0	DISABLE
						1	ENABLE
	9	CMP1BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
						1	ENABLE
	8	CMP1BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
						1	ENABLE
	7	CMP1AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at down counting	0	DISABLE
						1	ENABLE
	6	CMP1AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at up counting	0	DISABLE
						1	ENABLE
	5	CMP0BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at down counting	0	DISABLE
						1	ENABLE
	4	CMP0BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at up counting	0	DISABLE
						1	ENABLE
	3	CMP0AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at down counting	0	DISABLE
						1	ENABLE
	2	CMP0AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at up counting	0	DISABLE
						1	ENABLE
	1	PERIOD	RW	0x0	PWM trigger ADC signal when SAWCNT=Period	0	DISABLE
						1	ENABLE
	0	ZERO	RW	0x0	PWM trigger ADC signal when SAWCNT=Zero	0	DISABLE
						1	ENABLE
TRIG1CTL	0x0130	All		0x00000000	TRIG1 signal Control Register		
	31:29	EVTNUM	RW	0x0	PWM trigger event 1(TRIG1) number It indicates how many selected TRIG1 events have occurred. This field can be modified by firmware to adjust the phase of trigger sequence.	(x)	(x)
	28:27	Reserved	RO	0x0			
	26:24	EVTDIV	RW	0x0	PWM trigger event 1(TRIG1) divider select It determines how many selected TRIG1 events need to occur before a trigger pulse is generated.	(x)	ADD_ONE_(x)
	23:20	Reserved	RO	0x0			
	19	CMPTG2D	RW	0x0	PWM trigger ADC signal when TRIG2 event at down counting enable	0	DISABLE
						1	ENABLE

18	CMPTG2U	RW	0x0	PWM trigger ADC signal when TRIG2 event at up counting enable	0	DISABLE
					1	ENABLE
17	CMPTG1D	RW	0x0	PWM trigger ADC signal when TRIG1 event at down counting enable	0	DISABLE
					1	ENABLE
16	CMPTG1U	RW	0x0	PWM trigger ADC signal when TRIG1 event at up counting enable	0	DISABLE
					1	ENABLE
15	CMPTG0D	RW	0x0	PWM trigger ADC signal when TRIG0 event at down counting enable	0	DISABLE
					1	ENABLE
14	CMPTG0U	RW	0x0	PWM trigger ADC signal when TRIG0 event at up counting enable	0	DISABLE
					1	ENABLE
13	CMP2BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
					1	ENABLE
12	CMP2BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
					1	ENABLE
11	CMP2AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at down counting	0	DISABLE
					1	ENABLE
10	CMP2AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at up counting	0	DISABLE
					1	ENABLE
9	CMP1BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
					1	ENABLE
8	CMP1BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
					1	ENABLE
7	CMP1AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at down counting	0	DISABLE
					1	ENABLE
6	CMP1AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at up counting	0	DISABLE
					1	ENABLE
5	CMP0BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at down counting	0	DISABLE
					1	ENABLE
4	CMP0BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at up counting	0	DISABLE
					1	ENABLE
3	CMP0AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at down counting	0	DISABLE

						1	ENABLE
	2	CMP0AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at up counting	0	DISABLE
						1	ENABLE
	1	PERIOD	RW	0x0	PWM trigger ADC signal when SAWCNT=Period	0	DISABLE
						1	ENABLE
	0	ZERO	RW	0x0	PWM trigger ADC signal when SAWCNT=Zero	0	DISABLE
						1	ENABLE
TRIG2CTL	0x0134	All		0x00000000	TRIG2 signal Control Register		
	31:29	EVTNUM	RW	0x0	PWM trigger event 2(TRIG2) number It indicates how many selected TRIG2 events have occurred. This field can be modified by firmware to adjust the phase of trigger sequence.	(x)	(x)
	28:27	Reserved	RO	0x0			
	26:24	EVTDIV	RW	0x0	PWM trigger event 2(TRIG2) divider select It determines how many selected TRIG2 events need to occur before a trigger pulse is generated.	(x)	ADD_ONE_(x)
	23:20	Reserved	RO	0x0			
	19	CMPTG2D	RW	0x0	PWM trigger ADC signal when TRIG2 event at down counting enable	0	DISABLE
						1	ENABLE
	18	CMPTG2U	RW	0x0	PWM trigger ADC signal when TRIG2 event at up counting enable	0	DISABLE
						1	ENABLE
	17	CMPTG1D	RW	0x0	PWM trigger ADC signal when TRIG1 event at down counting enable	0	DISABLE
						1	ENABLE
	16	CMPTG1U	RW	0x0	PWM trigger ADC signal when TRIG1 event at up counting enable	0	DISABLE
						1	ENABLE
	15	CMPTG0D	RW	0x0	PWM trigger ADC signal when TRIG0 event at down counting enable	0	DISABLE
						1	ENABLE
	14	CMPTG0U	RW	0x0	PWM trigger ADC signal when TRIG0 event at up counting enable	0	DISABLE
						1	ENABLE
	13	CMP2BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
						1	ENABLE
	12	CMP2BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
						1	ENABLE
	11	CMP2AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at down counting	0	DISABLE
						1	ENABLE

	10	CMP2AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2A at up counting	0	DISABLE
						1	ENABLE
	9	CMP1BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at down counting	0	DISABLE
						1	ENABLE
	8	CMP1BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP2B at up counting	0	DISABLE
						1	ENABLE
	7	CMP1AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at down counting	0	DISABLE
						1	ENABLE
	6	CMP1AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP1A at up counting	0	DISABLE
						1	ENABLE
	5	CMP0BD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at down counting	0	DISABLE
						1	ENABLE
	4	CMP0BU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0B at up counting	0	DISABLE
						1	ENABLE
	3	CMP0AD	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at down counting	0	DISABLE
						1	ENABLE
	2	CMP0AU	RW	0x0	PWM trigger ADC signal when SAWCNT = CMP0A at up counting	0	DISABLE
						1	ENABLE
	1	PERIOD	RW	0x0	PWM trigger ADC signal when SAWCNT=Period	0	DISABLE
						1	ENABLE
	0	ZERO	RW	0x0	PWM trigger ADC signal when SAWCNT=Zero	0	DISABLE
						1	ENABLE
EVTFLG	0x0138	All		0x00000000	Trig and Interrupt Event Flag Register		
	31:11	Reserved	RO	0x0			
	10	TRIG2	W1C	0x0	Latched PWM ADC start-of-conversion B status flag. Write 1 clear	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	9	TRIG1	W1C	0x0	Latched PWM ADC start-of-conversion B status flag. Write 1 clear	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	TRIG0	W1C	0x0	Latched PWM trigger signal TRIG0 status flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7:1	Reserved	RO	0x0			
	0	INT	W1C	0x0	Latched PWM interrupt status flag. This bit is also the source of interrupt. New interrupt will not	0	NOT_OCCUR

					occur if this bit is not clear.		
						1	OCCUR\WRITE_1_CLEAR
EVTSWTRIG	0x013C	All		0x00000000	Event Software Trigger Register		
	31:11	Reserved	RO	0x0			
	10	TRIG2	W1S	0x0	Software trigger a TRIG2 event and auto clear to zero after setting.	0	NO_EFFECT
						1	ENABLE
	9	TRIG1	W1S	0x0	Software trigger a TRIG1 event and auto clear to zero after setting.	0	NO_EFFECT
						1	FORCE
	8	TRIG0	W1S	0x0	Software trigger a TRIG0 event and auto clear to zero after setting.	0	NO_EFFECT
						1	FORCE
	7:1	Reserved	RO	0x0			
	0	INT	W1S	0x0	Software trigger a INT event and auto clear to zero after setting.	0	NO_EFFECT
						1	FORCE

7.11 Direct Memory Access (DMA)

7.11.1 DMA Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
DMA_STS	0x0000	ALL		0x00000000	DMA status		
	31:29	Reserved	RO	0x0			
	28	TEST_STS	RO	0x0	To reduce the gate count you can configure the controller, to exclude the integration test logic.	0	NOT_INCLUDE_TEST_LOGIC
						1	INCLUDE_TEST_LOGIC
	27:18	Reserved	RO	0x0			
	17:16	CH_NUM	RO	0x0	Number of available DMA channels minus one	0	IS_CHANNEL_1
						1	IS_CHANNEL_2
						2	IS_CHANNEL_3
						3	IS_CHANNEL_4
	15:8	Reserved	RO	0x0			
	7:4	STATE	RO	0x0	Current state of the control state machine	0	IDLE
						1	READING_CONTROLLER_DATA
						2	READING_SOURCE_DATA_END_POINTER
						3	READING_DESTINATION_DATA_END_POINTER
						4	READING_SOURCE_DATA
						5	READING_DESTINATION_DATA
						6	WAITING_CONTROLLER_DATA
						7	WRITING_CONTROLLER_DATA
						8	STALLED
						9	DONE
						10	PERIPHERAL_TRANSITION
						11	RESERVED_0
						12	RESERVED_1
						13	RESERVED_2
						14	RESERVED_3
						15	RESERVED_4

	3:1	Reserved	RO	0x0			
	0	MASTER_EN_STS	RO	0x0	Pointer to the end address of the source data	0	IS_DISALED
						1	IS_ENABLED
DMA_CFG	0x0004	ALL		0x00000000	DMA configuration		
	31:8	Reserved	RO	0x0			
	7	HPROT_3	WO	0x0	Controls HPROT[3] to indicate if a cacheable access is occurring	0	SET_LOW
						1	SET_HIGH
	6	HPROT_2	WO	0x0	Controls HPROT[2] to indicate if a bufferable access is occurring	0	SET_LOW
						1	SET_HIGH
	5	HPROT_1	WO	0x0	Controls HPROT[1] to indicate if a privileged access is occurring.	0	SET_LOW
						1	SET_HIGH
	4:1	Reserved	RO	0x0			
	0	MASTER_EN	WO	0x0	Pointer to the end address of the source data	0	DISALE
						1	ENABLE
CTRL_BASE_PTR	0x0008	ALL		0x00000000	Channel Control data base pointer		
	31:7	CTRL_BASE_PTR	RO	0x0	You must configure this register so that the base pointer points to a location in your system memory.	(x)	(x)
	6:0	Reserved	RO	0x0	Undefined. Write as zero		
ALT_CTRL_BASE_PTR	0x000C	ALL		0x00000000	Channel alternate Control data base pointer		
	31:0	ALT_CTRL_BASE_PTR	RO	0x0	The read-only alt_ctrl_base_ptr Register returns the base address of the alternate data structure.	(x)	(x)
CH_WAITONREQ_STS	0x0010	ALL		0x00000000	Channel wait on request status Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RO	0x0	channel 4 wait on request status	0	IS_LOW
						1	IS_HIGH
	2	CH3	RO	0x0	channel 3 wait on request status	0	IS_LOW
						1	IS_HIGH
	1	CH2	RO	0x0	channel 2 wait on request status	0	IS_LOW
						1	IS_HIGH
	0	CH1	RO	0x0	channel 1 wait on request status	0	IS_LOW
						1	IS_HIGH
CH_SW_REQ	0x0014	ALL		0x00000000	Channel software request Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Set the appropriate bit to generate a software DMA request on the corresponding DMA 4 channel.	0	NOT_CREATE_REQUEST
						1	CREATE_REQUEST
	2	CH3	RW	0x0	Set the appropriate bit to generate a software DMA request on the corresponding DMA 3 channel.	0	NOT_CREATE_REQUEST
						1	CREATE_REQUEST
	1	CH2	RW	0x0	Set the appropriate bit to generate a software DMA request on the corresponding DMA 2 channel.	0	NOT_CREATE_REQUEST
						1	CREATE_REQUEST
	0	CH1	RW	0x0	Set the appropriate bit to generate a software DMA request on the corresponding DMA 1 channel.	0	NOT_CREATE_REQUEST

						1	CREATE_REQUEST
CH_USEBURST_SET	0x0018	ALL		0x00000000	Channel useburst set Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Returns the useburst status, or disables dma_sreq_4 from generating DMA requests	0	RESPOND_TO_REQ\NO_EFFECT
						1	NOT_RESPOND_TO_REQ\DISABLE_GENERATE_REQ
	2	CH3	RW	0x0	Returns the useburst status, or disables dma_sreq_3 from generating DMA requests	0	RESPOND_TO_REQ\NO_EFFECT
						1	NOT_RESPOND_TO_REQ\DISABLE_GENERATE_REQ
	1	CH2	RW	0x0	Returns the useburst status, or disables dma_sreq_2 from generating DMA requests	0	RESPOND_TO_REQ\NO_EFFECT
						1	NOT_RESPOND_TO_REQ\DISABLE_GENERATE_REQ
	0	CH1	RW	0x0	Returns the useburst status, or disables dma_sreq_1 from generating DMA requests	0	RESPOND_TO_REQ\NO_EFFECT
						1	NOT_RESPOND_TO_REQ\DISABLE_GENERATE_REQ
CH_USEBURST_CLR	0x001C	ALL		0x00000000	Channel useburst clear Register		
	31:8	Reserved	RO	0x0			
	3	CH4	WO	0x0	Set the appropriate bit to enable dma_sreq[] to generate requests	0	NO_EFFECT
						1	ENABLE_GENERATE_REQ
	2	CH3	WO	0x0	Set the appropriate bit to enable dma_sreq[] to generate requests	0	NO_EFFECT
						1	ENABLE_GENERATE_REQ
	1	CH2	WO	0x0	Set the appropriate bit to enable dma_sreq[] to generate requests	0	NO_EFFECT
						1	ENABLE_GENERATE_REQ
	0	CH1	WO	0x0	Set the appropriate bit to enable dma_sreq[] to generate requests	0	NO_EFFECT
						1	ENABLE_GENERATE_REQ
CH_REQ_MSK_SET	0x0020	ALL		0x00000000	Channel request mask set Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Returns the request mask status of dma_req[] and dma_sreq[], or disables the corresponding channel from generating DMA requests	0	IS_ENABLED\NO_EFFECT
						1	IS_DISABLED\DISABLE_DMA_REQ
	2	CH3	RW	0x0	Returns the request mask status of dma_req[] and dma_sreq[], or disables the corresponding channel from generating DMA requests	0	IS_ENABLED\NO_EFFECT
						1	IS_DISABLED\DISABLE_DMA_REQ
	1	CH2	RW	0x0	Returns the request mask status of dma_req[] and dma_sreq[], or disables the corresponding channel from generating DMA requests	0	IS_ENABLED\NO_EFFECT
						1	IS_DISABLED\DISABLE_DMA_REQ
	0	CH1	RW	0x0	Returns the request mask status	0	IS_ENABLED\NO_EFFECT

					of dma_req[] and dma_sreq[], or disables the corresponding channel from generating DMA requests		
						1	IS_DISABLED\DISABLE_DMA_REQ
CH_REQ_MSK_CLR	0x0024	ALL		0x00000000	Channel request mask clear Register		
	31:4	Reserved	RO	0x0			
	3	CH4	WO	0x0	Set the appropriate bit to enable DMA requests for the channel 4 corresponding to dma_req[] and dma_sreq[].	0	NO_EFFECT
						1	ENABLE_DMA_REQ
	2	CH3	WO	0x0	Set the appropriate bit to enable DMA requests for the channel 3 corresponding to dma_req[] and dma_sreq[].	0	NO_EFFECT
						1	ENABLE_DMA_REQ
	1	CH2	WO	0x0	Set the appropriate bit to enable DMA requests for the channel 2 corresponding to dma_req[] and dma_sreq[].	0	NO_EFFECT
						1	ENABLE_DMA_REQ
	0	CH1	WO	0x0	Set the appropriate bit to enable DMA requests for the channel 1 corresponding to dma_req[] and dma_sreq[].	0	NO_EFFECT
						1	ENABLE_DMA_REQ
CH_EN_SET	0x0028	ALL		0x00000000	Channel enable set Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Returns the enable status of the channels, or enables the corresponding channel 4	0	IS_DISABLED\NO_EFFECT
						1	IS_ENABLED\ENABLE
	2	CH3	RW	0x0	Returns the enable status of the channels, or enables the corresponding channel 3	0	IS_DISABLED\NO_EFFECT
						1	IS_ENABLED\ENABLE
	1	CH2	RW	0x0	Returns the enable status of the channels, or enables the corresponding channel 2	0	IS_DISABLED\NO_EFFECT
						1	IS_ENABLED\ENABLE
	0	CH1	RW	0x0	Returns the enable status of the channels, or enables the corresponding channel 1	0	IS_DISABLED\NO_EFFECT
						1	IS_ENABLED\ENABLE
CH_EN_CLR	0x002C	ALL		0x00000000	Channel enable clear Register		
	31:4	Reserved	RO	0x0			
	3	CH4	WO	0x0	Set the appropriate bit to disable the corresponding DMA channel4.	0	NO_EFFECT
						1	DISABLE
	2	CH3	WO	0x0	Set the appropriate bit to disable the corresponding DMA channel3.	0	NO_EFFECT
						1	DISABLE
	1	CH2	WO	0x0	Set the appropriate bit to disable the corresponding DMA channel2.	0	NO_EFFECT
						1	DISABLE
	0	CH1	WO	0x0	Set the appropriate bit to disable the corresponding DMA channel1.	0	NO_EFFECT
						1	DISABLE

CH_PRI_ALT_SET	0x0030	ALL		0x00000000	Channel primary-alternate set Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Returns the channel control data structure status, or selects the alternate data structure for the corresponding DMA channel4 .	0	USING_PRIMARY\NO_EFFECT
						1	USING_ALTERNATE\SELECT_ALTERNATE
	2	CH3	RW	0x0	Returns the channel control data structure status, or selects the alternate data structure for the corresponding DMA channel3.	0	USING_PRIMARY\NO_EFFECT
						1	USING_ALTERNATE\SELECT_ALTERNATE
	1	CH2	RW	0x0	Returns the channel control data structure status, or selects the alternate data structure for the corresponding DMA channel2.	0	USING_PRIMARY\NO_EFFECT
						1	USING_ALTERNATE\SELECT_ALTERNATE
	0	CH1	RW	0x0	Returns the channel control data structure status, or selects the alternate data structure for the corresponding DMA channel1.	0	USING_PRIMARY\NO_EFFECT
						1	USING_ALTERNATE\SELECT_ALTERNATE
CH_PRI_ALT_CLR	0x0034	ALL		0x00000000	Channel primary-alternate clear Register		
	31:4	Reserved	RO	0x0			
	3	CH4	WO	0x0	Set the appropriate bit to select the primary data structure for the corresponding DMA channel 4	0	NO_EFFECT
						1	SELECT_PRIMARY
	2	CH3	WO	0x0	Set the appropriate bit to select the primary data structure for the corresponding DMA channel 3	0	NO_EFFECT
						1	SELECT_PRIMARY
	1	CH2	WO	0x0	Set the appropriate bit to select the primary data structure for the corresponding DMA channel 2	0	NO_EFFECT
						1	SELECT_PRIMARY
	0	CH1	WO	0x0	Set the appropriate bit to select the primary data structure for the corresponding DMA channel 1	0	NO_EFFECT
						1	SELECT_PRIMARY
CH_PRIORITY_SET	0x0038	ALL		0x00000000	Channel priority set Register		
	31:4	Reserved	RO	0x0			
	3	CH4	RW	0x0	Returns the channel 4 priority mask status, or sets the channel 4 priority to high	0	USING_DEFAULT_LEVEL\NO_EFFECT
						1	USING_HIGH_LEVEL\SELECT_HIGH_LEVEL
	2	CH3	RW	0x0	Returns the channel 3 priority mask status, or sets the channel 3 priority to high	0	USING_DEFAULT_LEVEL\NO_EFFECT
						1	USING_HIGH_LEVEL\SELECT_HIGH_LEVEL
	1	CH2	RW	0x0	Returns the channel 2 priority mask status, or sets the channel 2 priority to high	0	USING_DEFAULT_LEVEL\NO_EFFECT
						1	USING_HIGH_LEVEL\SELECT_HIGH_LEVEL
	0	CH1	RW	0x0	Returns the channel 1 priority	0	USING_DEFAULT_LEVEL\

					mask status, or sets the channel 1 priority to high		NO_EFFECT
						1	USING_HIGH_LEVEL\SELECT_HIGH_LEVEL
CH_PRIORITY_CLR	0x003C	ALL		0x00000000	Channel priority clear Register		
	31:4	Reserved	RO	0x0			
	3	CH4	WO	0x0	Set the appropriate bit to select the default priority level for the specified DMA channel 4	0	NO_EFFECT
						1	SELECT_DEFAULT_LEVEL
	2	CH3	WO	0x0	Set the appropriate bit to select the default priority level for the specified DMA channel 3	0	NO_EFFECT
						1	SELECT_DEFAULT_LEVEL
	1	CH2	WO	0x0	Set the appropriate bit to select the default priority level for the specified DMA channel 2	0	NO_EFFECT
						1	SELECT_DEFAULT_LEVEL
	0	CH1	WO	0x0	Set the appropriate bit to select the default priority level for the specified DMA channel 1	0	NO_EFFECT
						1	SELECT_DEFAULT_LEVEL
Reserved	0x0040	All	RO				
	31:0	Reserved	RO	0x0			
BUS_ERR_CLR	0x004C	ALL		0x00000000	Bus error clear Register		
	31:1	Reserved	RO	0x0			
	0	ERR_CLR	RW	0x0	Returns the status of dma_err, or sets the signal LOW.	0	NO_EFFECT
						1	SET_DMA_ERR_LOW

7.12 Flexible Memory Controller (FMC)

7.12.1 FMC Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	Label
FITST	0x0000	All		0x00000000	Flash Inter Setting register		
	31:1	Reserved	RO	0x0			
	0	EMBF_EN	RW	0x0	The interrupt is asserted to CPU when the cmd_mode command is done.	0	DISABLE
						1	ENABLE
FCMD	0x0004	All		0x00000000	Flash Commands register		
	31:5	Reserved	RO	0x0			
	4	DEEP_STDBY	RW	0x0	Write '1' to make embedded flash IP get into deep standby state. write cmd_mode bit before writing this bit.	0	IS_DONE
						1	IS_BUSY
	3	RESET	RW	0x0	Write '1' to start embedded flash IP reset. write cmd_mode bit before writing this bit.	0	IS_DONE
						1	IS_BUSY
	2	CHIP_ERASE	RW	0x0	Write '1' to do chip erase. write cmd_mode bit before writing this bit.	0	IS_DONE
						1	IS_BUSY
	1	PWR_OFF	RW	0x0	Write '1' to turn on the embedded flash IP VDD. The cmd_reset timing is followed soon after power on	0	IS_DONE
						1	IS_BUSY

	0	PWR_ON	RW	0x0	Write '1' to turn on the embedded flash IP VDD	0	IS_DONE
						1	IS_BUSY
FPROGT	0x0008	All		0x00000002	Flash programming type register		
	31:2	Reserved	RO	0x0			
	1:0	EMBF_EN	RW	0x2	The flash programming type selector. 2'b01 is for row based, 2'b10 is for sector based, other values are of single word, single short, and single byte programming.	0	SINGLE_PROGRAMMING_0
						1	ROW_BASED
						2	SECTOR_BASED
						3	SINGLE_PROGRAMMING_3
FSTS	0x000C	All		0x00000000	Flash programming type register		
	31:1	Reserved	RO	0x0			
	2	HV_TIMEOUT	RO	0x0	High voltage for a row programming timeout.		
	1	EMBF_RDY	RO	0x0	embedded flash controller is in idle state and ready for access.		
	0	EMBF_INTR_STS	W1C	0x0	interrupt status. Write '1' to clear.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
Reserved	0x0010	All		0x00000000			
	31:0	Reserved	RO	0x0			
FBNK1WRP	0x0018	All		0x00000001	Flash Bank 1 write protect register		
	31:1	Reserved	RO	0x0			
	0	BANK_1_WR_PROT	RW	0x1	set s_acc_key to 'h0F72630C to enable write access right to this bit bank1 is the region of 0x00010c00 to 0x000117 .	0	UNLOCK
						1	LOCK
Reserved	0x001C	All		0x00000000			
	31:0	Reserved	RO	0x0			
FBNKUWRP	0x0020	All		0x00000001	Flash Bank U write protect register		
	31:1	Reserved	RO	0x0			
	0	BANK_U_WR_PROT	RW	0x1	set s_acc_key to 'h0F495469 to enable write access right to this bit. bank user is the region of 0x00000000 to 0x00010000 .	0	UNLOCK
						1	LOCK
Reserved	0x0024	All		0x00000000			
	31:0	Reserved	RO	0x0			
FBNK1RDP	0x002C	All		0x00000001	Flash Bank 1 Read Protect Register		
	31:1	Reserved	RO	0x0			
	0	BANK_1_RD_PROT	RW	0x1	set s_acc_key to 'h0C0F7263 to enable write access right to this bit. bank1 is the region of 0x00010c00 to 0x000117ff .	0	UNLOCK
						1	LOCK
Reserved	0x0030	All		0x00000000			
	31:0	Reserved	RO	0x0			
FKEY	0x0034	All		0x00000000	Flash keys Register		
	31:0	FLS_ACC_KEY	RO	0x0	Flash key	(x)	(x)
FSTRERS	0x010C	All		0x00000000	Flash Sector Erase Register		
	31:1	Reserved	RO	0x0			
	0	CMD_SECTOR_ERASE	RW	0x0	Write '1' to do sector erase according to cfg_A. Read '1' when busy. Read '0' when done.	0	IS_DONE
						1	IS_BUSY\DO_SECTOR_ERASE
FRDADDPOR	0x0110	All		0x00000000	Flash read address port Register		
	31:17	Reserved	RO	0x0			

	16:0	RD_A	RW	0x0	read mode address. Be noted that it is of byte address and is aligned with word (32-bit) address. The NVR sector selector is defined by rd_A[17]=1. That is, the NVR sector is at the space above 128KB.	(x)	(x)
FRDDATPOR	0x0114	All		0x00000000	Flash read data port Register		
	31:0	CMD_LATCH_DOUT	RW	0x0	Auto latched DOUT[31:0] according to the embedded flash IP timing. The flash read is started by writing flash address value to the rd_A register. The result is latched in the cmd_latch_DOUT register. The result is valid when the embf_rdy bit is '1'.	(x)	(x)
FWRADDPOR	0x0118	All		0x00000000	Flash write address port Register		
	31:17	Reserved	RO	0x0			
	16:0	CFG_A	RW	0x0	The cfg_A is used for sector erase and programming. Be noted that it is of byte address from software point of view. The address is aligned with 512-byte address when used as sector erase address. It is the starting address of the programming process. It is aligned with word (32-bit) address for programming. The NVR sector selector is defined by cfg_A[17]=1. That is, the NVR sector is at the space above 128KB.	(x)	(x)
FWRNADDPOR	0x011C	All		0x00000000	Flash next address for write Register		
	31:17	Reserved	RO	0x0			
	16:0	CMD_NEXT_A	RW	0x0	command mode next address. Be noted that it is of byte address and aligned with word (32-bit) address. When the cfg_DIN Is programmed done, the cmd_next_A is the next address to be programmed. On polling the change of the cmd_next_A, the host can write the new cfg_DIN for the next word programming.	(x)	(x)
FWRDATPOR	0x0120	All		0x00000000	Flash write data port Register		
	31:0	CFG_DIN	RW	0x0	command mode write data. Write this register will start a word programming according to cfg_A, cmd_next_A and cfg_DIN contents. The NVR sector selector is defined by cfg_A[17]=1. The programming is done on the 512-byte sector o set. tHV (8ms) rule time out monitor is automatically enabled. Please read the bit HV_timeout after the programming is done.	(x)	(x)

7.13 Global Module Setting (GLOBAL)

The GLOBAL Module has three functions. The first function is for two input signals to do logic operation, as shown in Figure 7-8. The second function is to create a window filter for MTPWM Brake, which is shown in

Figure 7-9. The last function is to generate a synchronous signal for MTPWM and ETIMER module, the control logic and multiplexer connection is shown in Figure 7-10.

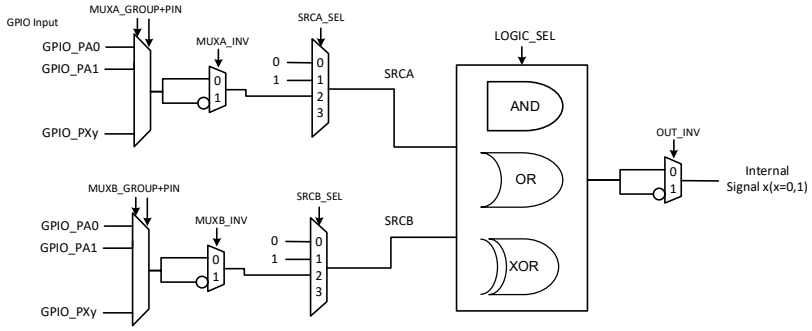


Figure 7-8 GLOBAL Logic Block Circuit

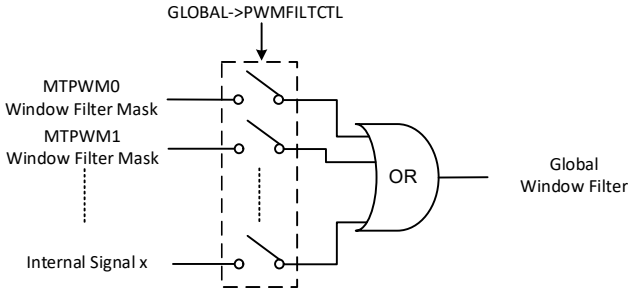


Figure 7-9 GLOBAL MTPWM Window Filter

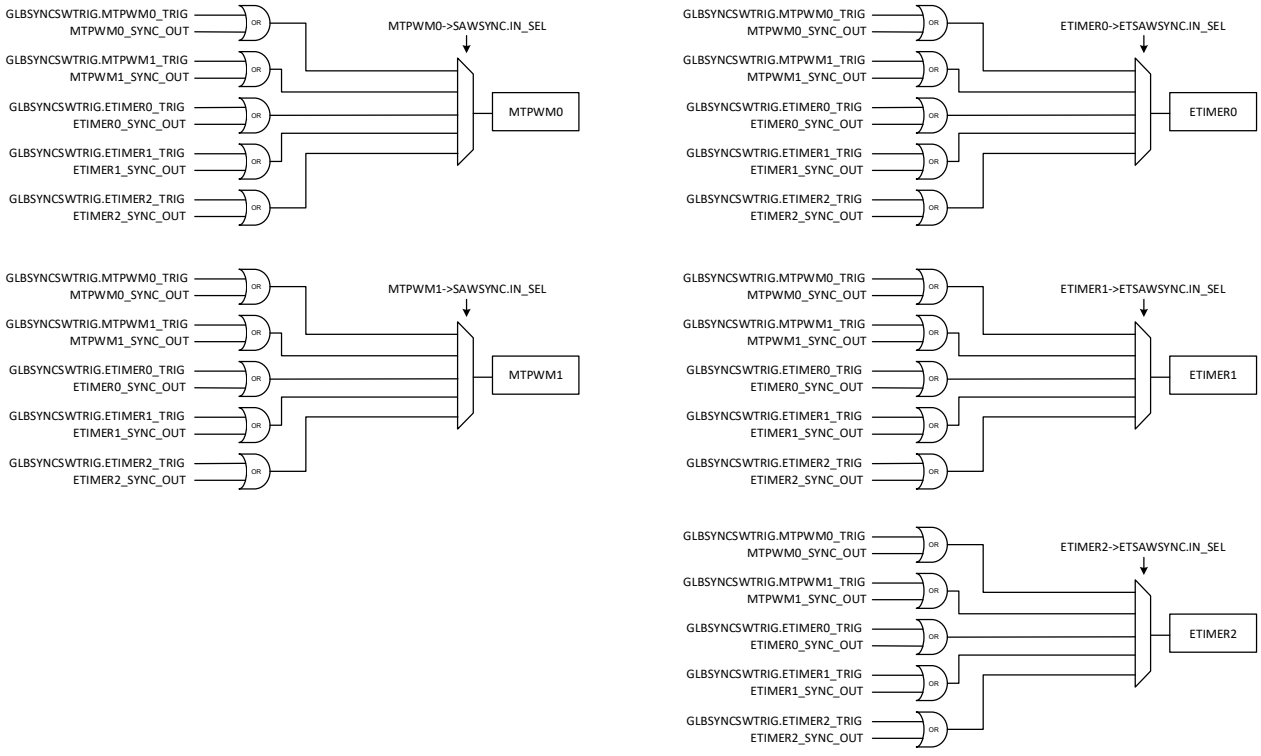


Figure 7-10 GLOBAL Synchronous Signal Diagram

7.13.1 GLOBAL Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
INSIG0CTL	0x0000	All		0x00000000	Internal Signal 0 Control Register		
	31:27	Reserved	RO	0x0			
	26	OUTINV	RW	0x0	Output inverter selection	0	DISABLE
						1	ENABLE
	25:24	LOGIC_SEL	RW	0x0	Select logic operation action of source A and B	0	AND
						1	OR
						2	XOR
						3	RESERVED
	23:21	Reserved	RO	0x0			
	20:19	SRCB	RW	0x0	Source B Selection	0	AS_LOW
						1	AS_HIGH
						2	FROM_MUXB
						3	RESERVED
	18	MUXB_INV	RW	0x0	MUXB Output with inverter	0	DISABLE
						1	ENABLE
	17	Reserved	RO	0x0			
	16:15	MUXB_GROUP	RW	0x0	MUX B GPIO Group	0	PA_GROUP
						1	PB_GROUP
						2	PC_GROUP
						3	RESERVED
	14:11	MUXB_PIN	RW	0x0	Select Pin in GPIO Group defined by MUXA_GROUP	(x)	(x)
	10	Reserved	RO	0x0			
	9:8	SRCA_SEL	RW	0x0	Source A Selection	0	AS_LOW
						1	AS_HIGH
						2	FROM_MUXA
						3	RESERVED
	7	MUXA_INV	RW	0x0	MUXA Output with inverter	0	DISABLE
						1	ENABLE
	6	Reserved	RO	0x0			
	5:4	MUXA_GROUP	RW	0x0	MUX A GPIO Group	0	PA_GROUP
						1	PB_GROUP
						2	PC_GROUP
						3	RESERVED
	3:0	MUXA_PIN	RW	0x0	Select Pin in GPIO Group defined by MUXA_GROUP	(x)	(x)
INSIG1CTL	0x0004	All		0x00000000	Internal Signal 1 Control Register		
	31:27	Reserved	RO	0x0			
	26	OUTINV	RW	0x0	Output inverter selection	0	DISABLE
						1	ENABLE
	25:24	LOGIC_ACT	RW	0x0	Select logic operation action of source A and B	0	AND
						1	OR
						2	XOR
						3	RESERVED
	23:21	Reserved	RO	0x0			
	20:19	SRCB	RW	0x0	Source B Selection	0	AS_LOW
						1	AS_HIGH
						2	FROM_MUXB
						3	RESERVED
	18	MUXB_INV	RW	0x0	MUXB Output with inverter	0	DISABLE
						1	ENABLE
	17	Reserved	RO	0x0			
	16:15	MUXB_GROUP	RW	0x0	MUX B GPIO Group	0	PA_GROUP
						1	PB_GROUP
						2	PC_GROUP
						3	RESERVED
	14:11	MUXB_PIN	RW	0x0	Select Pin in GPIO Group defined	(x)	(x)

					by MUXA_GROUP		
	10	Reserved	RO	0x0			
	9:8	SRCA_SEL	RW	0x0	Source A Selection	0	AS_LOW
						1	AS_HIGH
						2	FROM_MUXA
						3	RESERVED
	7	MUXA_INV	RW	0x0	MUXA Output with inverter	0	DISABLE
						1	ENABLE
	6	Reserved	RO	0x0			
	5:4	MUXA_GROUP	RW	0x0	MUX A GPIO Group	0	PA_GROUP
						1	PB_GROUP
						2	PC_GROUP
						3	RESERVED
	3:0	MUXA_PIN	RW	0x0	Select Pin in GPIO Group defined by MUXA_GROUP	(x)	(x)
Reserved	0x0008	All	RO				
	31:0	Reserved	RO	0x0			
ISIGSTSFLG	0x0020	All		0x00000000	Internal Signal Status Flag Register		
	31:18	Reserved	RO	0x0			
	17	SIG1_STS	RO	0x0	Internal signal 1 status	0	LEVEL_LOW
						1	LEVEL_HIGH
	16	SIG0_STS	RO	0x0	Internal signal 0 status	0	LEVEL_LOW
						1	LEVEL_HIGH
	15:10	Reserved	RO	0x0			
	9	SIG1_FALLING	W1C	0x0	Internal signal 1 rising edge flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	SIG0_FALLING	W1C	0x0	Internal signal 0 rising edge flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7:2	Reserved	RO	0x0			
	1	SIG1_RISING	W1C	0x0	Internal signal 1 rising edge flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	SIG0_RISING	W1C	0x0	Internal signal 0 rising edge flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
Reserved	0x0024	All	RO				
	31:0	Reserved	RO	0x0			
PWMFILTCTL	0x0040	All		0x00000000	MTPWM Window Filter Global Combination Control Register		
	31:4	Reserved	RO	0x0			
	3	ISIG1_EN	RW	0x0	Internal signal 1 as input	0	DISABLE
						1	ENABLE
	2	ISIG0_EN	RW	0x0	Internal signal 0 as input	0	DISABLE
						1	ENABLE
	1	MTPWM1_EN	RW	0x0	Select MTPWM1 Window as input	0	DISABLE
						1	ENABLE
	0	MTPWM0_EN	RW	0x0	Select MTPWM0 Window as input	0	DISABLE
						1	ENABLE
Reserved	0x0044	All	RO				
	31:0	Reserved	RO	0x0			
GLBSYNCSWTRIG	0x0060	All		0x00000000	Global Force Sync Signal Generate Register		
	31:11	Reserved	RO	0x0			
	10	ETIMER2_TRIG	W1S	0x0	Force hardware to generate a sync signal to module	0	NO_EFFECT
						1	ENABLE
	9	ETIMER1_TRIG	W1S	0x0	Force hardware to generate a sync signal to module	0	NO_EFFECT
						1	ENABLE
	8	ETIMER0_TRIG	W1S	0x0	Force hardware to generate a sync signal to module	0	NO_EFFECT
						1	ENABLE
	7:2	Reserved	RO	0x0			
	1	MTPWM1_TRIG	W1S	0x0	Force hardware to generate a	0	NO_EFFECT

					sync signal to module		
						1	ENABLE
	0	MTPWM0_TRIG	W1S	0x0	Force hardware to generate a sync signal to module	0	NO_EFFECT
						1	ENABLE
Reserved	0x0064	All	RO				
	31:0	Reserved	RO	0x0			
COMDAT0	0x0100	ALL		0x560000AA	Simply RW for communication or virtual hardware.		
	31:0	VAL	RW	0x560000AA	Data stored	(x)	(x)
COMDAT1	0x0104	ALL		0x00000000	Simply RW for communication or virtual hardware.		
	31:0	VAL	RW	0x0	Data stored	(x)	(x)
COMDAT2	0x0108	ALL		0x00000000	Simply RW for communication or virtual hardware.		
	31:0	VAL	RW	0x0	Data stored	(x)	(x)
COMDAT3	0x010C	ALL		0x00000000	Simply RW for communication or virtual hardware.		
	31:0	VAL	RW	0x0	Data stored	(x)	(x)

7.14 Dual Timer (DUALTIMER)

7.14.1 DUALTIMER Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
LD1	0x0000	ALL		0x00000000	LOAD register 1		
	31:0	LD1	RW	0x0	The Current value register is also overwritten if the BGLD1 is written to and the current count is immediately affected.	(x)	(x)
VAL1	0x0004	ALL		0xFFFFFFFF	Current Value register 1		
	31:0	VAL1	RO	0xFFFFFFFF	the current value of the decrementing counter	(x)	(x)
CTL1	0x0008	ALL		0x00000020	Timer Control register 1		
	31:8	Reserved	RO	0x0		(x)	(x)
	7	TIM_EN	RW	0x0	Timer Enable	0	DISABLE
						1	ENABLE
	6	MODE	RW	0x0	Timer Mode change	0	FREE_RUNNING_MODE
						1	PERIODIC_MODE
	5	IRQ_EN	RW	0x0	Timer Interrupt Enable	0	DISABLE
						1	ENABLE
	4	Reserved	RO	0x0			
	3:2	PRESCALE	RW	0x0	Prescale	0	DIV_BY_1
						1	DIV_BY_16
						2	DIV_BY_256
						3	DO_NOT_USE
	1	SIEZ	RW	0x0	Selects 16-bit or 32-bit counter operation:	0	16_BIT_COUNTER
						1	32_BIT_COUNTER
	0	ONESHOT	RW	0x0	Selects one-shot or wrapping counter mode:	0	WRAPPING_MODE
						1	ONE_SHOT_MODE
IRCR1	0x000C	ALL		0x00000000	Interrupt Clear register 1		
	31:0	CLR	RW	0x0	any write to clear register	(x)	(x)
RIRST1	0x0010	ALL		0x00000000	Raw Interrupt Status register 1		
	31:1	Reserved	RO	0x0			
	0	RAWIRQ	RO	0x0	This value is ANDed with the timer interrupt enable bit from the Timer Control register to create the masked interrupt, that is passed to the interrupt output pin	0	NOT_OCCUR
						1	OCCUR
IRST1	0x0014	ALL		0x00000000	Interrupt Status register 1		
	31:1	Reserved	RO	0x0			

	0	MASKIRQ	RO	0x0	This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control register, and is the same value that is passed to the interrupt output pin	0	NOT_OCCUR
						1	OCCUR
BGLD1	0x0018	ALL		0x00000000	Background Load register 1		
	31:0	BGLD1	RW	0x0	The Current value register is also overwritten if the BGLD1 is written to, but the current count is not immediately affected.	(x)	(x)
Reserved	0x001C	All		0x00000000			
	31:0	Reserved	RO	0x0			
LD2	0x0020	ALL		0x00000000	LOAD register 2		
	31:0	LD1	RW	0x0	This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control register, and is the same value that is passed to the interrupt output pin	(x)	(x)
VAL2	0x0024	ALL		0xFFFFFFFF	Current Value register 2		
	31:0	VAL1	RO	0xFFFFFFFF	the current value of the decrementing counter	(x)	(x)
CTL2	0x0028	ALL		0x00000000	Timer Control register 2		
	31:8	Reserved	RO	0x0			
	7	TIM_EN	RW	0x0	Timer Enable	0	DISABLE
						1	ENABLE
	6	TIM_EN	RW	0x0	Timer Mode change	0	FREE_RUNNING_MODE
						1	PERIODIC_MODE
	5	IRQ_EN	RW	0x0	Timer Interrupt Enable	0	DISABLE
						1	ENABLE
	4	Reserved	RO	0x0			
	3:2	PRESCALE	RW	0x0	Prescale	0	DIV_BY_1
						1	DIV_BY_16
						2	DIV_BY_256
						3	DO_NOT_USE
	1	SIEZ	RW	0x0	Selects 16-bit or 32-bit counter operation:	0	16_BIT_COUNTER
						1	32_BIT_COUNTER
	0	ONESHOT	RW	0x0	Selects one-shot or wrapping counter mode:	0	WRAPPING_MODE
						1	ONE_SHOT_MODE
IRCR2	0x002C	ALL		0x00000000	Interrupt Clear register 2		
	31:0	CLR	RW	0x0	any write to clear register	(x)	(x)
RIRST2	0x0030	ALL		0x00000000	Raw Interrupt Status register 2		
	31:1	Reserved	RO	0x0			
	0	RAWIRQ	RO	0x0	This value is ANDed with the timer interrupt enable bit from the Timer Control register to create the masked interrupt, that is passed to the interrupt output pin	0	NOT_OCCUR
						1	OCCUR
IRST2	0x0034	ALL		0x00000000	Interrupt Status register 2		
	31:1	Reserved	RO	0x0			
	0	MASKIRQ	RO	0x0	This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control register, and is the same value that is passed to the interrupt output pin	0	NOT_OCCUR
						1	OCCUR
BGLD2	0x0038	ALL		0x00000000	Background Load register 1		
	31:0	BGLD2	RW	0x0	The Current value register is also overwritten if the BGLD1 is written to, but the current count	(x)	(x)

					is not immediately affected.		

7.15 Analog Circuit Setting (ANALOG)

7.15.1 ANALOG Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
ANACTL	0x0000	All		0x00000000	ANALOG Control Register		
	31:4	Reserved	RO	0x0			
	3	DEBUG_BUFF	RW	0x0		0	DISABLE
						1	ENABLE
	2	DAC10B	RW	0x0		0	DISABLE
						1	ENABLE
	1	Reserved	RO	0x0			
	0	DAC6B	RW	0x0		0	DISABLE
						1	ENABLE
DAC10BVAL	0x0004	All		0x00000000	10-Bit DAC Data Register		
	31:10	Reserved	RO	0x0			
	9:0	VAL	RW	0x0	DAC 10 bit value register	(x)	(x)
DAC6BVAL	0x0008	All	Protect	0x00000000	6-Bit DAC Data Register		
	31:14	Reserved	RO	0x0			
	13:8	VAL1	RW	0x0	DAC 6 bit value register 1	(x)	(x)
	7:6	Reserved	RO	0x0			
	5:0	VAL0	RW	0x0	DAC 6 bit value register 0	(x)	(x)
Reserved	0x000C	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
DEBUGSEL	0x0010	All		0x00000000	Debug Buffer Output Select Register		
	31:4	Reserved	RO	0x0			
	3:0	MUXSEL	RW	0x0		0	PGA0_O
						1	PGA1_O
						2	PGA2_O
						3	PGA3_O
						4	DAC_10BIT
						5	DAC_6BIT_0
						6	DAC_6BIT_1
						7	VREF
						8	VCOM
						9	RESERVED
						10	RESERVED
						11	BAND_GAP
						12	PLL_VCO
						13	RESERVED
						14	RESERVED
						15	RESERVED
VREFSEL	0x0014	All		0x00000000	VREF Select Register		
	31:2	Reserved	RO	0x0			
	1:0	MUXSEL	RW	0x0		0	FROM_AVDD
						1	FROM_4096MV
						2	FROM_2560MV
						3	FROM_EXT_PIN

7.16 Analog Comparator (ACOMP)

The FP5600 contains 4 Analog Comparators (ACOMP) which can be used in many different configurations. When the positive input is greater than the negative input, the ACOMP output is logic 1, otherwise the output is 0. Each ACOMP can be configured to generate an interrupt when the ACOMP output

value changes.

ACOMP includes a programmable hysteresis function with 4 hysteresis levels (20, 40, 80, 120 mV).

The debounce filter in the ACOMP block is similar to the input debounce filter in the GPIO block. ACOMP's debounce filter control has 10-bit control steps to provide various ranges of noise filtering.

FP5600 ACOMP0~3 channel configuration is shown in Figure 7-11.

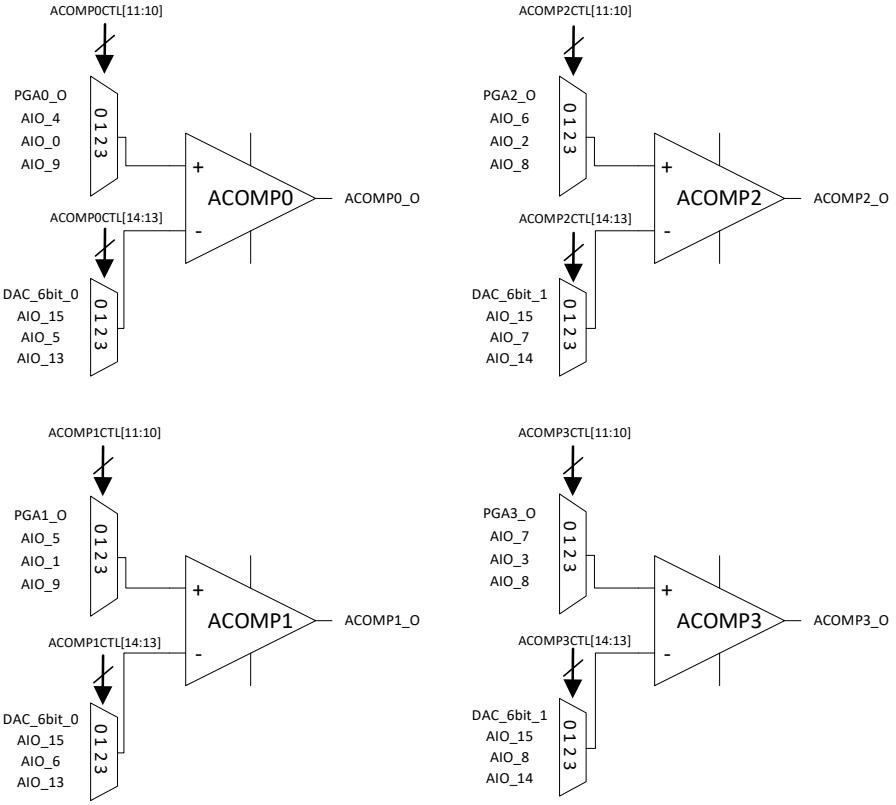


Figure 7-11 ACOMP channel selection

7.5.1 ACOMP Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
ACOMP0CTL	0x0000	All		0x00000000	ACOMP0 Control Register		
	31:26	Reserved	RO	0x0			
	25:16	FILT_NUM	RW	0x0	Output Debounce Filter Width (10 bit)	(x)	CONTI_SAMPLE_(x)
	15	Reserved	RO	0x0			
	14:13	CHN_SEL	RW	0x0	Negative Channel Selection	0	DAC_6BIT_0
						1	AIO_15
						2	AIO_5
						3	AIO_13
	12	Reserved	RO	0x0			
	11:10	CHP_SEL	RW	0x0	Positive Channel Selection	0	PGA0_O
						1	AIO_4

						2	AIO_0
						3	AIO_9
	9:8	INT_TYPE	RW	0x0	Interrupt type selection	0	DISABLE
						1	RISING_EDGE
						2	FALLING_EDGE
						3	BOTH_EDGE
	7:4	HYST_SEL	RW	0x0	Interrupt type selection	1	20MV
						2	40MV
						4	80MV
						8	120MV
	3	Reserved	RO	0x0			
	2	FILT_EN	RW	0x0	Output Debounce Filter Enable	0	DISABLE
						1	ENABLE
	1	INV	RW	0x0	Output Inverter	0	DISABLE
						1	ENABLE
	0	EN	RW	0x0	Enable Analog Comparator0	0	DISABLE
						1	ENABLE
ACOMP1CTL	0x0004	All		0x00000000	ACOMP1 Control Register		
	31:26	Reserved	RO	0x0			
	25:16	FILT_NUM	RW	0x0	Output Debounce Filter Width(10 bit)	(x)	CONTI_SAMPLE_(x)
	15	Reserved	RO	0x0			
	14:13	CHN_SEL	RW	0x0	Negative Channel Selection	0	DAC_6BIT_0
						1	AIO_15
						2	AIO_6
						3	AIO_13
	12	Reserved	RO	0x0			
	11:10	CHP_SEL	RW	0x0	Positive Channel Selection	0	PGA1_O
						1	AIO_5
						2	AIO_1
						3	AIO_9
	9:8	INT_TYPE	RW	0x0	Interrupt type selection	0	DISABLE
						1	RISING_EDGE
						2	FALLING_EDGE
						3	BOTH_EDGE
	7:4	HYST_SEL	RW	0x0	Hysteresis Level Selection	1	20MV
						2	40MV
						4	80MV
						8	120MV
	3	Reserved	RO	0x0			
	2	FILT_EN	RW	0x0	Output Debounce Filter Enable	0	DISABLE
						1	ENABLE
	1	INV	RW	0x0	Output Inverter	0	DISABLE
						1	ENABLE
	0	EN	RW	0x0	Enable Analog Comparator0	0	DISABLE
						1	ENABLE
ACOMP2CTL	0x0008	All		0x00000000	ACOMP2 Control Register		
	31:26	Reserved	RO	0x0			

	25:16	FILT_NUM	RW	0x0	Output Debounce Filter Width(10 bit)	(x)	CONTI_SAMPLE_(x)
	15	Reserved	RO	0x0			
	14:13	CHN_SEL	RW	0x0	Negative Channel Selection	0	DAC_6BIT_1
						1	AIO_15
						2	AIO_7
						3	AIO_14
	12	Reserved	RO	0x0			
	11:10	CHP_SEL	RW	0x0	Positive Channel Selection	0	PGA2_O
						1	AIO_6
						2	AIO_2
						3	AIO_8
	9:8	INT_TYPE	RW	0x0	Interrupt type selection	0	DISABLE
						1	RISING_EDGE
						2	FALLING_EDGE
						3	BOTH_EDGE
	7:4	HYST_SEL	RW	0x0	Hysteresis Level Selection	1	20MV
						2	40MV
						4	80MV
						8	120MV
	3	Reserved	RO	0x0			
	2	FILT_EN	RW	0x0	Output Debounce Filter Enable	0	DISABLE
						1	ENABLE
	1	INV	RW	0x0	Output Inverter	0	DISABLE
						1	ENABLE
	0	EN	RW	0x0	Enable Analog Comparator0	0	DISABLE
						1	ENABLE
ACOMP3CTL	0x000C	All		0x00000000	ACOMP3 Control Register		
	31:26	Reserved	RO	0x0			
	25:16	FILT_NUM	RW	0x0	Output Debounce Filter Width(10 bit)	(x)	CONTI_SAMPLE_(x)
	15	Reserved	RO	0x0			
	14:13	CHN_SEL	RW	0x0	Negative Channel Selection	0	DAC_6BIT_1
						1	AIO_15
						2	AIO_8
						3	AIO_14
	12	Reserved	RO	0x0			
	11:10	CHP_SEL	RW	0x0	Positive Channel Selection	0	PGA3_O
						1	AIO_7
						2	AIO_3
						3	AIO_8
	9:8	INT_TYPE	RW	0x0	Interrupt type selection	0	DISABLE
						1	RISING_EDGE
						2	FALLING_EDGE
						3	BOTH_EDGE
	7:4	HYST_SEL	RW	0x0	Hysteresis Level Selection	1	20MV
						2	40MV

						4	80MV
						8	120MV
	3	Reserved	RO	0x0			
	2	FILT_EN	RW	0x0	Output Debounce Filter Enable	0	DISABLE
						1	ENABLE
	1	INV	RW	0x0	Output Inverter	0	DISABLE
						1	ENABLE
	0	EN	RW	0x0	Enable analog comparator	0	DISABLE
						1	ENABLE
STSFLG	0x0010	All		0x00000000	Output flag of analog comparator and interrupt		
	31:12	Reserved	RO	0x0			
	11	CMP3STS	RO	0x0	The output of analog comparator 3(non-latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	10	CMP2STS	RO	0x0	The output of analog comparator 2(non-latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	9	CMP1STS	RO	0x0	The output of analog comparator 1(non-latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	8	CMP0STS	RO	0x0	The output of analog comparator 0(non-latched)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	7:4	Reserved	RO	0x0			
	3	CMP3INTFLG	W1C	0x0	COMP3 Interrupt Flag(Write 1 Clear)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	2	CMP2INTFLG	W1C	0x0	COMP2 Interrupt Flag(Write 1 Clear)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	CMP1INTFLG	W1C	0x0	COMP1 Interrupt Flag(Write 1 Clear)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	CMP0INTFLG	W1C	0x0	COMP0 Interrupt Flag(Write 1 Clear)	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR

7.17 Programmable Gain Amplifier (PGA)

The FP5600 contains a Programmable Gain Amplifier (PGA) as Figure 7-12. The user can measure the output of the programmable gain amplifier to the integrated ADC channel, and obtain the digital result there. Additionally, users can adjust the gain to 1, 2, 4, 8, 16 and 32.

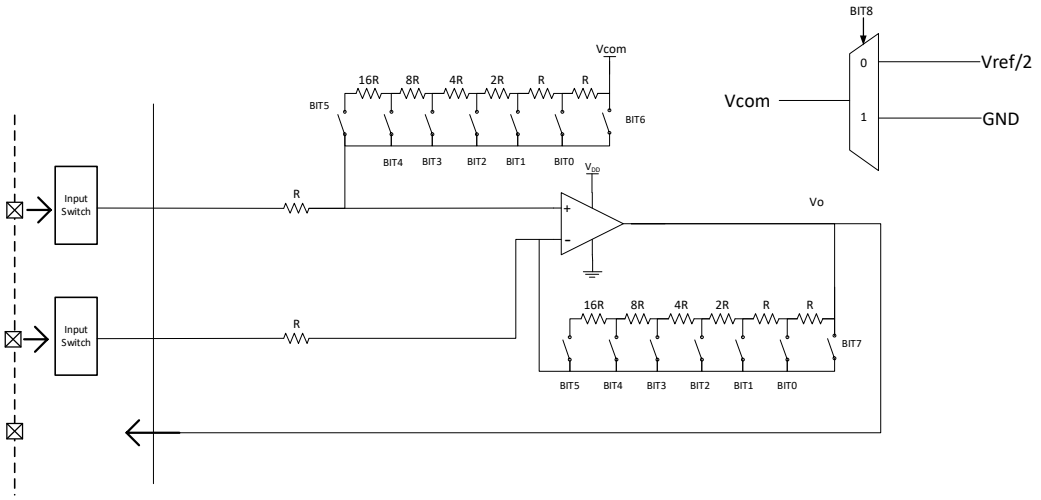


Figure 7-12 PGA structure

FP5600 PGA0~3 channel configuration is shown in Figure 7-13.

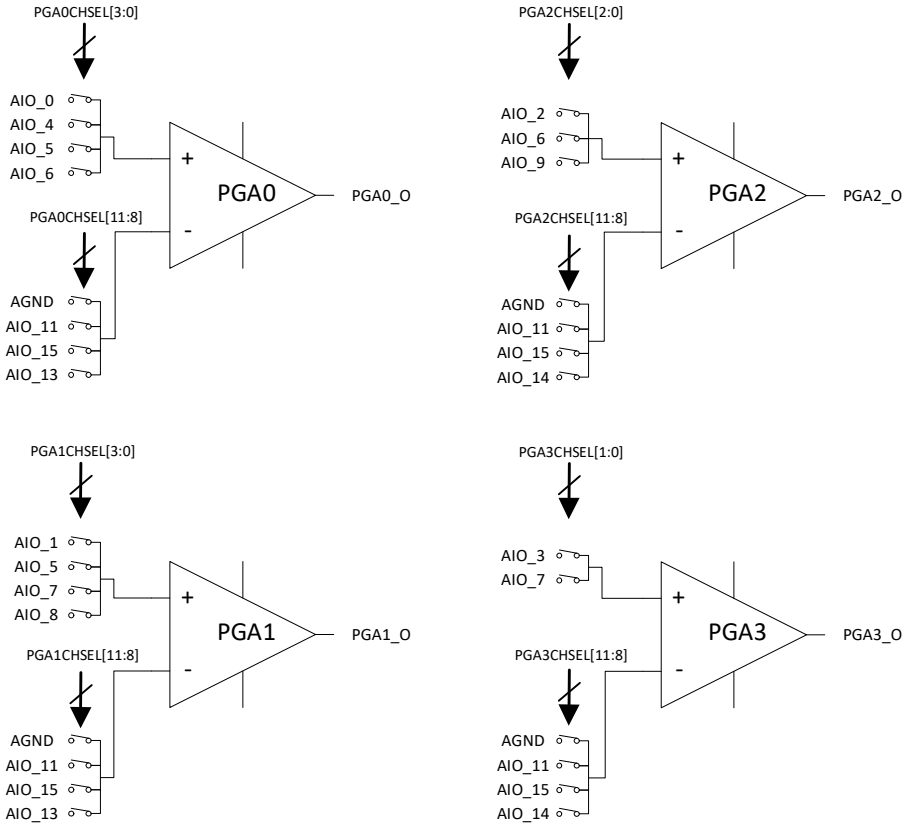


Figure 7-13 PGA channel selection

7.17.1 PGA Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
PGA0CTL	0x0000	ALL		0x00000000	PGA0 Control Register		

	31:22	Reserved	RO	0x0			
	21	EN	RW	0x0	Module Enable	0	DISABLE
						1	ENABLE
	20:9	Reserved	RO	0x0			
	8	VCOM_SEL	RW	0x0	Common Mode Voltage Selection	0	VREF_OVER_2
						1	GND
	7	ON_SHORT	RW	0x0	Short OP Output to Negative Input	0	DISABLE
						1	ENABLE
	6	LVL_SHORT	RW	0x0	Level Shift Switch Selection.	0	DISABLE
						1	ENABLE
	5:0	R_LVL	RW	0x0	Level Shift Resistor Network Selection	0	AS_OPEN
						1	AS_R
						2	AS_2R
						4	AS_4R
						8	AS_8R
						16	AS_16R
						32	AS_32R
PGA0CHSEL	0x0004	ALL		0x00000000	PGA0 Input Channel Select Register		
	31:12	Reserved	RO	0x0			
	11	N_AIO_13	RW	0x0		0	DISABLE
						1	ENABLE
	10	N_AIO_15	RW	0x0	Debug out, for DAC usage.	0	DISABLE
						1	ENABLE
	9	N_AIO_11	RW	0x0		0	DISABLE
						1	ENABLE
	8	N_AGND	RW	0x0		0	DISABLE
						1	ENABLE
	7:4	Reserved	RO	0x0			
	3	P_AIO_6	RW	0x0		0	DISABLE
						1	ENABLE
	2	P_AIO_5	RW	0x0		0	DISABLE
						1	ENABLE
	1	P_AIO_4	RW	0x0		0	DISABLE
						1	ENABLE
	0	P_AIO_0	RW	0x0		0	DISABLE
						1	ENABLE
Reserved	0x0008	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
Reserved	0x000C	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
PGA1CTL	0x0010	ALL		0x00000000	PGA1 Control Register		
	31:22	Reserved	RO	0x0			
	21	EN	RW	0x0	Module Enable	0	DISABLE
						1	ENABLE
	20:9	Reserved	RO	0x0			
	8	VCOM_SEL	RW	0x0	Common Mode Voltage Selection	0	VREF_OVER_2
						1	GND
	7	ON_SHORT	RW	0x0	Short OP Output to Negative Input	0	DISABLE
						1	ENABLE
	6	LVL_SHORT	RW	0x0	Level Shift Switch Selection.	0	DISABLE
						1	ENABLE
	5:0	R_LVL	RW	0x0	Level Shift Resistor Network Selection	0	AS_OPEN
						1	AS_R
						2	AS_2R

						4	AS_4R
						8	AS_8R
						16	AS_16R
						32	AS_32R
PGA1CHSEL	0x0014	ALL		0x00000000	PGA1 Input Channel Select Register		
	31:12	Reserved	RO	0x0			
	11	N_AIO_13	RW	0x0		0	DISABLE
						1	ENABLE
	10	N_AIO_15	RW	0x0	Debug out, for DAC usage.	0	DISABLE
						1	ENABLE
	9	N_AIO_11	RW	0x0		0	DISABLE
						1	ENABLE
	8	N_AGND	RW	0x0		0	DISABLE
						1	ENABLE
	7:5	Reserved	RO	0x0			
	3	P_AIO_8	RW	0x0		0	DISABLE
						1	ENABLE
	2	P_AIO_7	RW	0x0		0	DISABLE
						1	ENABLE
	1	P_AIO_5	RW	0x0		0	DISABLE
						1	ENABLE
	0	P_AIO_1	RW	0x0		0	DISABLE
						1	ENABLE
Reserved	0x0018	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
Reserved	0x001C	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
PGA2CTL	0x0020	ALL		0x00000000	PGA2 Control Register		
	31:22	Reserved	RO	0x0			
	21	EN	RW	0x0	Module Enable	0	DISABLE
						1	ENABLE
	20:9	Reserved	RO	0x0			
	8	VCOM_SEL	RW	0x0	Common Mode Voltage Selection	0	VREF_OVER_2
						1	GND
	7	ON_SHORT	RW	0x0	Short OP Output to Negative Input	0	DISABLE
						1	ENABLE
	6	LVL_SHORT	RW	0x0	Level Shift Switch Selection.	0	DISABLE
						1	ENABLE
	5:0	R_LVL	RW	0x0	Level Shift Resistor Network Selection	0	AS_OPEN
						1	AS_R
						2	AS_2R
						4	AS_4R
						8	AS_8R
						16	AS_16R
						32	AS_32R
PGA2CHSEL	0x0024	ALL		0x00000000	PGA2 Input Channel Select Register		
	31:12	Reserved	RO	0x0			
	11	N_AIO_14	RW	0x0		0	DISABLE
						1	ENABLE
	10	N_AIO_15	RW	0x0	Debug out, for DAC usage.	0	DISABLE
						1	ENABLE
	9	N_AIO_11	RW	0x0		0	DISABLE
						1	ENABLE
	8	N_AGND	RW	0x0		0	DISABLE
						1	ENABLE

	7:5	Reserved	RO	0x0			
	2	P_AIO_9	RW	0x0		0	DISABLE
						1	ENABLE
	1	P_AIO_6	RW	0x0		0	DISABLE
						1	ENABLE
	0	P_AIO_2	RW	0x0		0	DISABLE
						1	ENABLE
Reserved	0x0028	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
Reserved	0x002C	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
PGA3CTL	0x0030	ALL		0x00000000	PGA3 Control Register		
	31:22	Reserved	RO	0x0			
	21	EN	RW	0x0	Module Enable	0	DISABLE
						1	ENABLE
	20:9	Reserved	RO	0x0			
	8	VCOM_SEL	RW	0x0	Common Mode Voltage Selection	0	VREF_OVER_2
						1	GND
	7	ON_SHORT	RW	0x0	Short OP Output to Negative Input	0	DISABLE
						1	ENABLE
	6	LVL_SHORT	RW	0x0	Level Shift Switch Selection.	0	DISABLE
						1	ENABLE
	5:0	R_LVL	RW	0x0	Level Shift Resistor Network Selection	0	AS_OPEN
						1	AS_R
						2	AS_2R
						4	AS_4R
						8	AS_8R
						16	AS_16R
						32	AS_32R
PGA3CHSEL	0x0034	ALL		0x00000000	PGA3 Input Channel Select Register		
	31:12	Reserved	RO	0x0			
	11	N_AIO_14	RW	0x0		0	DISABLE
						1	ENABLE
	10	N_AIO_15	RW	0x0	Debug out, for DAC usage.	0	DISABLE
						1	ENABLE
	9	N_AIO_11	RW	0x0		0	DISABLE
						1	ENABLE
	8	N_AGND	RW	0x0		0	DISABLE
						1	ENABLE
	7:2	Reserved	RO	0x0			
	1	P_AIO_7	RW	0x0		0	DISABLE
						1	ENABLE
	0	P_AIO_3	RW	0x0		0	DISABLE
						1	ENABLE
Reserved	0x0038	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
Reserved	0x003C	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
ANACTL	0x0040	ALL		0x00000000	Analog Control Register		
	31:1	Reserved	RO	0x0			
	0	VOCM_EN	RW	0x0		0	DISABLE
						1	ENABLE

7.18 Clock Setting (CLOCK)

The clock controller generates clocks for the entire chip, including system clocks and peripheral clocks. The clock controller also implements power control functions with individual clock on/off controls, clock source selection, and clock dividers. Only when the SLEEPMODE_EN (CLOCK->PWRCTL[2]) bit is set to 1, the chip will enter Sleep Mode. After that, the chip enters Sleep Mode and waits for GPIO wake-up trigger to exit power-down mode. In Sleep Mode, the clock controller turns off the 4~20 MHz external high-speed crystal oscillator (HXT) and the 48MHz high-speed internal RC oscillator (HIRC) to reduce overall system power consumption. Figure 7-14 and Figure 7-15 show an overview of the clock generator and clock source control.

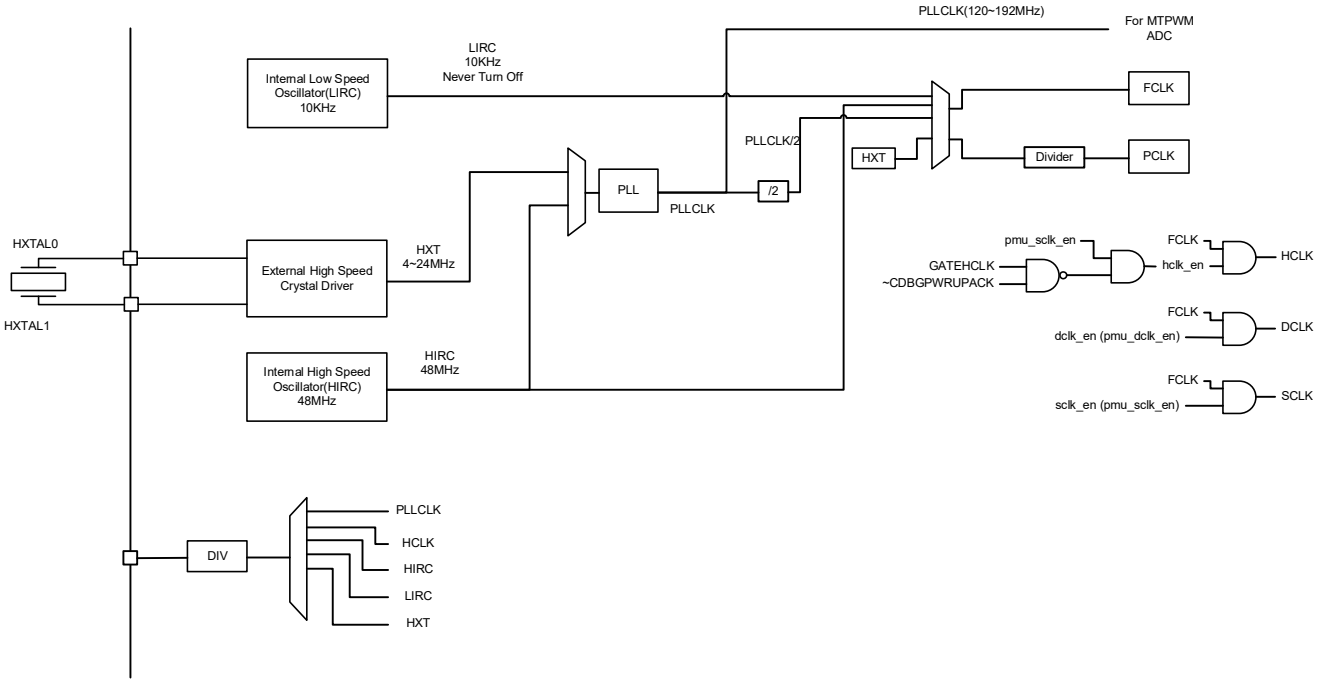


Figure 7-14 System Clock Tree

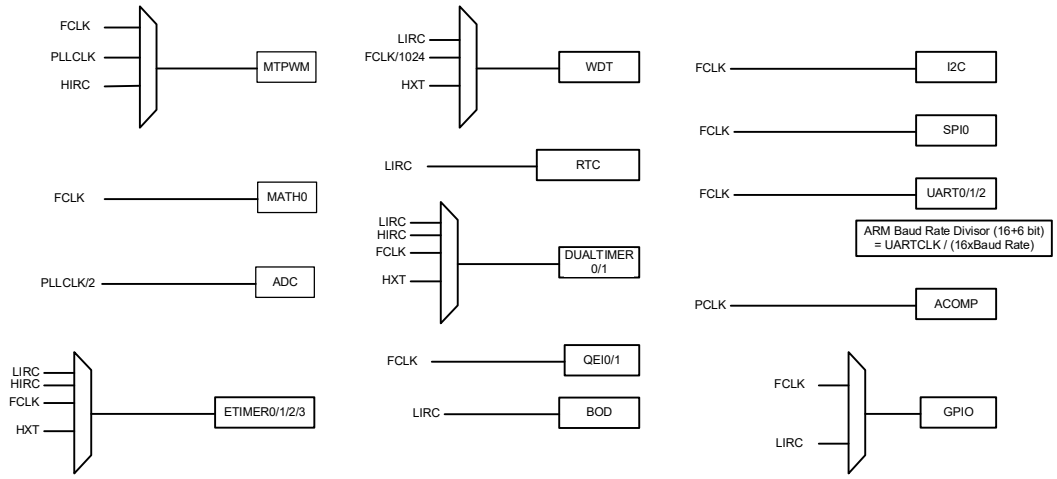


Figure 7-15 Module Clock Tree

7.18.1 CLOCK Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
PWRCTL	0x0000	All	Protect	0x00000000	Power Mode Control Register		

	31:8	Reserved	RO	0x0			
	7:4	SLEEPMODE_MASK	RW	0x0	Sleep Mode Input PAD Mask	0	DISABLE
						1	PA2_MASK
						2	PA9_MASK
						4	PA12_MASK
						8	PB1_MASK
	3	Reserved	RO	0x0			
	2	SLEEPMODE_EN	RW	0x0	System Sleep Enable Control (Write Protect) Refer to the SYS->UNLOCK register. When this bit is set to 1, Sleep mode is enabled. When chip wakes up from Sleep mode, this bit is auto cleared. Users need to set this bit again for next Sleep. In Sleep mode, HXT and HIRC will be disabled. In Sleep mode, the system clocks are disabled, and ignored the clock source selection. The clocks of peripheral are not controlled by Sleep mode if the peripheral clock source is from LIRC. LIRC is controlled by bit LIRCEN.	0	DISABLE
						1	ENABLE
	1	SLEEPWAK_INTFLG	W1C	0x0	Sleep Mode Wake-up Interrupt Flag Set by “Sleep wake-up event”, it indicates that resume from “Sleep mode” The flag is set if the GPIO wake-up occurred. Note1: Write 1 to clear the bit to 0. Note2: This bit works only if SLEEPWAK_INTEN (SLEEPCTL[0]) set to 1.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	SLEEPWAK_INTEN	RW	0x0	Sleep Mode Wake-up Interrupt Enable Control (Write Protect) Refer to the SYS->UNLOCK register.	0	DISABLE
						1	ENABLE
CLKCTL	0x0004	All	Protect	0x00000100	Clock Control Register		
	31:9	Reserved	RO	0x0			
	8	HIRC_EN	RO	0x1	HIRC enables the control system to automatically stay high when the system wakes up	0	DISABLE
						1	ENABLE
	7:2	Reserved	RO	0x0			
	1	HXT_MODE	RW	0x0	HXT Bypass/Normal Control (Write Protect) Refer to the SYS->UNLOCK register.	0	NORMAL_MODE
						1	BYPASS_MODE
	0	HXT_EN	RW	0x0	HXT Enable Control (Write Protect) Refer to the SYS->UNLOCK register.	0	DISABLE
						1	ENABLE
PLLCTL	0x0008	All	Protect	0x00000082	PLL Control Register		
	31:18	Reserved	RO	0x0			
	17	PLL_CK_SEL	RW	0x0		0	FROM_INTERNAL_CLOCK
						1	FROM_EXTERNAL_CLOCK

	16	PLL_LOCKM	RW	0x0		0	VCOCLK_CHECK_UNLOCK
						1	OSC_CHECK_UNLOCK
	15	PLL_EN	RW	0x0	PLL Enable Register	0	DISABLE
						1	ENABLE
	14	PLL_LOCK	RO	0x0	A/D signal, dynamic, debounce 32T(PLL_CK_SEL).	0	
						1	
	13:11	PLL_TM	RW	0x0	PLL test mode	(x)	(x)
	10:4	PLL_SEL_N	RW	0x8	PLL N	(x)	(x)
	3:0	PLL_SEL_M	RW	0x2	PLL M	(x)	(x)
SYSCLKSEL	0x000C	All		0x00000000	System Clock Selection Register		
	31:3	Reserved	RO	0x0			
	2	PCLK_SEL	RW	0x0	PCLK Source Selection	0	FROM_FCLK_DIV_1
						1	FROM_FCLK_DIV_2
	1:0	FCLK_SEL	RW	0x0	FCLK Source Selection	0	FROM_HIRC
						1	FROM_LIRC
						2	FROM_PLL
						3	FROM_HXT
STSFLG	0x0010	All		0x00000000	Clock Stable Status Monitor Register		
	31:3	Reserved	RO	0x0			
	2	PLL_STABLE	RO	0x0		0	NOT_READY
						1	READY
	1	HIRC_STABLE	RO	0x0	HIRC Clock Source Stable Status (Read Only, non-latched) 0 = 48 MHz internal high speed RC oscillator (HIRC) clock is not stable or disabled. 1 = 48 MHz internal high speed RC oscillator (HIRC) clock is stable and enabled.	0	NOT_READY
						1	READY
	0	LIRC_STABLE	RO	0x0	LIRC Clock Source Stable Status (Read Only, non-latched) 0 = 10 kHz internal low speed RC oscillator (LIRC) clock is not stable or disabled. 1 = 10 kHz internal low speed RC oscillator (LIRC) clock is stable and enabled.	0	NOT_READY
						1	READY
CLKOCTL	0x0014	All		0x00000000	Clock Output Control Register		
	31:25	Reserved	RO	0x0			
	24	CLKOEN	RW	0x0	Clock Output Enable Control	0	OUT_DISABLE
						1	OUT_ENABLE
	23:19	Reserved	RO	0x0			
	18:16	CLKO_SRC	RW	0x0	Clock Divider Clock Source Selection	0	FROM_LIRC
						1	HIRC
						2	PLL
						3	HXT
						4	HCLK
						5	Reserved
						6	Reserved
						7	Reserved
	15:8	Reserved	RO	0x0			
	7:0	DIV	RW	0x0	Clock Output Frequency Selection The formula of output frequency is Fout= Fin/(2*N).	(x)	POWER_OF_2N
APBMODEN0	0x0018	All		0x00000000	APB Bus Module Clock Enable Register 0		

31:28	Reserved	RO	0x0			
27	CRC_EN	RW	0x0	CRC Module Clock Enable Register	0	DISABLE
					1	ENABLE
26	PGA_EN	RW	0x0	PGA Module Clock Enable Register	0	DISABLE
					1	ENABLE
25	ACOMP_EN	RW	0x0	ACMP(Analog Comparator) Module Clock Enable Register	0	DISABLE
					1	ENABLE
24	ANALOG_EN	RW	0x0	Analog Module Clock Enable Register	0	DISABLE
					1	ENABLE
23	DMA_EN	RW	0x0	DMA Module Clock Enable Register	0	DISABLE
					1	ENABLE
22	MTPWM1_EN	RW	0x0	MTPWM1 Module Clock Enable Register	0	DISABLE
					1	ENABLE
21	MTPWM0_EN	RW	0x0	MTPWM0 Module Clock Enable Register	0	DISABLE
					1	ENABLE
20	QEI1_EN	RW	0x0	QEI1 Module Clock Enable Register	0	DISABLE
					1	ENABLE
19	QEI0_EN	RW	0x0	QEI0 Module Clock Enable Register	0	DISABLE
					1	ENABLE
18	GLOBAL_EN	RW	0x0	Global Module Enable Register	0	DISABLE
					1	ENABLE
17	ETIMER2_EN	RW	0x0	ETimer2 Module Clock Enable Register	0	DISABLE
					1	ENABLE
16	ETIMER1_EN	RW	0x0	ETimer1 Module Clock Enable Register	0	DISABLE
					1	ENABLE
15	ETIMER0_EN	RW	0x0	ETimer0 Module Clock Enable Register	0	DISABLE
					1	ENABLE
14	Reserved	RO	0x0			
13	TIMER1_EN	RW	0x0	Timer1 Module Clock Enable Register	0	DISABLE
					1	ENABLE
12	TIMER0_EN	RW	0x0	Timer0 Module Clock Enable Register	0	DISABLE
					1	ENABLE
11	ADC_EN	RW	0x0	ADC Module Clock Enable Register	0	DISABLE
					1	ENABLE
10	RTC_EN	RW	0x0	RTC Module Clock Enable Register	0	DISABLE
					1	ENABLE
9	WDT_EN	RW	0x0	WDT Module Clock Enable Register	0	DISABLE
					1	ENABLE
8	Reserved	RO	0x0			
7	I2C0_EN	RW	0x0	I2C0 Module Clock Enable Register	0	DISABLE
					1	ENABLE
6	SPI0_EN	RW	0x0	SPI0 Module Clock Enable Register	0	DISABLE
					1	ENABLE

	5:3	Reserved	RO	0x0			
	2	UART2_EN	RW	0x0	UART2 Module Clock Enable Register	0	DISABLE
						1	ENABLE
	1	UART1_EN	RW	0x0	UART1 Module Clock Enable Register	0	DISABLE
						1	ENABLE
	0	UART0_EN	RW	0x0	UART0 Module Clock Enable Register	0	DISABLE
						1	ENABLE
AHBMODEN0	0x001C	All	Protect	0x00000000	AHB Bus Module Clock Enable Register 0		
	31:14	Reserved	RO	0x0			
	13	HDIV_EN	RW	0x0	HDIV Module Clock Enable Register	0	DISABLE
						1	ENABLE
	12	CORDIC_EN	RW	0x0	CORDIC Module Clock Enable Register	0	DISABLE
						1	ENABLE
	11:9	Reserved	RO	0x0			
	8	GPIOC_EN	RW	0x0	CPIO Group C Module Clock Enable Register	0	DISABLE
						1	ENABLE
	7	GPIOB_EN	RW	0x0	CPIO Group B Module Clock Enable Register	0	DISABLE
						1	ENABLE
	6	GPIOA_EN	RW	0x0	CPIO Group A Module Clock Enable Register	0	DISABLE
						1	ENABLE
	5:0	Reserved	RO	0x0			
TIMER0CTL	0x0020	All		0x00000000	TIMER0 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	TIMER0 Clock Source Selection	0	FROM_LIRC
						1	FROM_HIRC
						2	FROM_FCLK
						3	FROM_HXT
TIMER1CTL	0x0024	All		0x00000000	TIMER1 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	TIMER1 Clock Source Selection	0	FROM_LIRC
						1	FROM_HIRC
						2	FROM_FCLK
						3	FROM_HXT
ETIMER0CTL	0x0028	All		0x00000000	ETIMER1 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	ETIMER1 Clock Source Selection	0	FROM_LIRC
						1	FROM_HIRC
						2	FROM_FCLK
						3	FROM_HXT
ETIMER1CTL	0x002C	All		0x00000000	ETIMER2 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	ETIMER2 Clock Source Selection	0	FROM_LIRC
						1	FROM_HIRC
						2	FROM_FCLK
						3	FROM_HXT
ETIMER2CTL	0x0030	All		0x00000000	ETIMER3 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	ETIMER3 Clock Source Selection	0	FROM_LIRC
						1	FROM_HIRC
						2	FROM_FCLK
						3	FROM_HXT

WDTCTL	0x0034	All	Protect	0x00000000	WDT Clock Control Register This register is protected by SYS->UNLOCK		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	WDT Clock Source Selection	0	FROM_LIRC
						1	FROM_FCLK_DIV_1024
						2	FROM_HXT
						3	Reserved
MTPWM0CTL	0x0038	All		0x00000000	MTPWM0 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	MTPWM0 Clock Source Selection	0	FROM_FCLK
						1	FROM_PLL
						2	FROM_HIRC
						3	Reserved
MTPWM1CTL	0x003C	All		0x00000000	MTPWM1 Clock Control Register		
	31:2	Reserved	RO	0x0			
	1:0	SRC	RW	0x0	MTPWM0 Clock Source Selection	0	FROM_FCLK
						1	FROM_PLL
						2	FROM_HIRC
						3	Reserved

7.19 System (SYS)

7.19.1 SYS Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
BODCTL	0x0000	ALL	Protect	0x00000000	BOD Control Register (Write Protect) Refer to the SYS->UNLOCK register.		
	31:7	Reserved	RO	0x0			
	6	BOD_OUT	RO	0x0	Brown-out Detector Output Status	0	HIGHER_THAN_BODVL
						1	LOWER_THAN_BODVL
	5	BOD_INTFLG	W1C	0x0	Brown-out Detector Interrupt Flag Note: Write 1 to clear this bit to 0.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	4	BOD_RSTEN	RW	0x0	Brown-out Reset Enable Control (Write Protect) Refer to the SYS->UNLOCK register.	0	DISABLE
						1	ENABLE
	3:1	BOD_LEVEL	RW	0x0	Brown-out Detector Threshold Voltage Selection (Write Protect) Refer to the SYS->UNLOCK register.	0	BOD_LEVEL_2V3
						1	BOD_LEVEL_2V6
						2	BOD_LEVEL_2V9
						3	BOD_LEVEL_3V2
						4	BOD_LEVEL_3V5
						5	BOD_LEVEL_3V8
						6	BOD_LEVEL_4V1
						7	BOD_LEVEL_4V4
	0	BOD_EN	RW	0x0	Brown-out Detector Enable Control (Write Protect) Refer to the SYS->UNLOCK register.	0	DISABLE
						1	ENABLE
PDID	0x0004	All		0x56000001	Part Device Identification Number Register		
	31:0	VAL	RO	0x56000001	This register reflects device part	(x)	(x)

					number code. Software can read this register to identify which device is used.		
RSTFLG	0x0008	All		0x00000000	System Reset Flag Register. This register cannot be reset by any reset quest. (Write Protect) Refer to the SYS->UNLOCK register.		
	31:19	Reserved	RO	0x0			
	18	ESD_5V0	W1C	0x0	ESD 5V Flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	17	ESD_1V5	W1C	0x0	ESD 1.5V Flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	16	OTP	W1C	0x0	Over Temperature Protection Flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	15:13	Reserved	RO	0x0			
	12	LOCKUP	W1C	0x0	M0+ core lock up flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	11	HARDFAULT	W1C	0x0	Hard Fault Flag	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	10:6	Reserved	RO	0x0			
	5	SYSTEM	W1C	0x0	System Reset Flag The system reset flag is set by the "Reset Signal" from the Cortex -M0+ Core to indicate the previous reset source.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	4	BOD	W1C	0x0	BOD Reset Flag The BOD reset flag is set by the "Reset Signal" from the Brown-Out Detector to indicate the previous reset source.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	3	Reserved	RO	0x0			
	2	WDT	W1C	0x0	WDT Reset Flag The WDT reset flag is set by the "Reset Signal" from the Watchdog Timer to indicate the previous reset source.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	1	NRST_PIN	W1C	0x0	NRST Pin Reset Flag The nRST pin reset flag is set by the "Reset Signal" from the nRST Pin to indicate the previous reset source.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
	0	POR	W1C	0x0	POR Reset Flag The POR reset flag is set by the "Reset Signal" from the Power-on Reset (POR) Controller or bit CHIP_RST (SYS->SRST.CHIP_RST) to indicate the previous reset source.	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR
SRST	0x000C	All	Protect	0x00000000	System Reset Register 0(Auto clear) (Write Protect) Refer to the SYS->UNLOCK register.		
	31:1	Reserved	RO	0x0			
	0	CHIP_RST	W1S	0x0	Setting this bit will reset the whole chip, including Processor core and all peripherals, and this bit will automatically return to 0 after the 2 clock cycles (CPUCLK). The CHIPRST is same as the POR reset, all the chip controllers is reset and the chip setting from	0	NORMAL_WORK

					flash are also reload.		
						1	PULSE_ENABLE
APBRST	0x0010	All	Protect	0x00000000	APB Bus Module Software Reset Register (Auto clear) All bitfield in this register are all write protect. Refer to the SYS->UNLOCK register.		
	31:28	Reserved	RO	0x0			
	27	CRC_RST	W1S	0x0	CRC Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	26	PGA_RST	W1S	0x0	PGA Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	25	ACOMP_RST	W1S	0x0	ACOMP(Analog Comparator) Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	24	ANALOG_RST	W1S	0x0	Analog Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	23	DMA_RST	W1S	0x0	DMA Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	22	MTPWM1_RST	W1S	0x0	MTPWM1 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	21	MTPWM0_RST	W1S	0x0	MTPWM0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	20	QEI1_RST	W1S	0x0	QEI1 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	19	QEI0_RST	W1S	0x0	QEI0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	18	GLOBAL_RST	W1S	0x0	Global Module Reset Register	0	DISABLE
						1	ENABLE
	17	ETIMER2_RST	W1S	0x0	ETIMER 2 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	16	ETIMER1_RST	W1S	0x0	ETIMER 1 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	15	ETIMER0_RST	W1S	0x0	ETIMER 0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	14	Reserved	RO	0x0			
	13	TIMER1_RST	W1S	0x0	Timer1 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	12	TIMER0_RST	W1S	0x0	Timer0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	11	ADC_RST	W1S	0x0	ADC Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	10	RTC_RST	W1S	0x0	RTC Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	9	WDT_RST	W1S	0x0	WDT Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	8	Reserved	RO	0x0			
	7	I2C0_RST	W1S	0x0	I2C0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	6	SPI0_RST	W1S	0x0	SPI0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	5:3	Reserved	RO	0x0			
	2	UART2_RST	W1S	0x0	UART2 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	1	UART1_RST	W1S	0x0	UART1 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
	0	UART0_RST	W1S	0x0	UART0 Module Reset Register	0	NORMAL_WORK
						1	ENABLE
Reserved	0x0014	All	Protect	0x00000000	Reserved		
	31:0	Reserved	RO	0x0			
AHBRST	0x0018	All	Protect	0x00000000	AHB Bus Module Reset Register (Auto clear) All bitfield in this register are all write protect. Refer to the		

					SYS->UNLOCK register.		
	31:14	Reserved	RO	0x0			
	13	HDIV_RST	W1S	0x0	HDIV Module Reset Register	0	DISABLE
						1	ENABLE
	12	CORDIC_RST	W1S	0x0	CORDIC Module Reset Register	0	DISABLE
						1	ENABLE
	11:9	Reserved	RO	0x0			
	8	GPIOC_RST	W1S	0x0	CPIO Group C Module Reset Register	0	DISABLE
						1	ENABLE
	7	GPIOB_RST	W1S	0x0	CPIO Group B Module Reset Register	0	DISABLE
						1	ENABLE
	6	GPIOA_RST	W1S	0x0	CPIO Group A Module Reset Register	0	DISABLE
						1	ENABLE
	5:3	Reserved	RO	0x0			
	2	SYS_RST	W1S	0x0	SYS Module Reset Register	0	DISABLE
						1	ENABLE
	1:0	Reserved	RO	0x0			
DMASEL	0x001C	All	Protect	0x00000000	DMA Module Selection Register		
	31:2	Reserved	RO	0x0			
	7:6	DMA_CH4_SEL	RW	0x0	DMA Channel 4 Selection	0	Reserved
						1	I2C0_TX
						2	UART0_RX
						3	UART1_RX
	5:4	DMA_CH3_SEL	RW	0x0	DMA Channel 3 Selection	0	SPI0_TX
						1	I2C0_RX
						2	UART0_TX
						3	UART1_TX
	3:2	DMA_CH2_SEL	RW	0x0	DMA Channel 2 Selection	0	SPI0_RX
						1	Reserved
						2	UART0_TX
						3	UART2_RX
	1:0	DMA_CH1_SEL	RW	0x0	DMA Channel 1 Selection	0	Reserved
						1	UART0_RX
						2	UART2_TX
						3	Reserved
DMAWAITONREQ	0x0020	All	Protect	0x00000000	DMA Wait on Request Register		
	31:10	Reserved	RO	0x0			
	9	DMA_Manual_SREQ	WO	0x0	DMA_Manual_SREQ Write Kick		
	8	DMA_Manual_REQ	WO	0x0	DMA_Manual_REQ Write Kick		
	7:5	Reserved	RO	0x0			
	4	DMA_STALL	RW	0x0	DMA_STALL		
	3	CH4	RW	0x0	Chanel 4 wait on request enable bit	0	DISABLE
						1	ENABLE
	2	CH3	RW	0x0	Chanel 3 wait on request enable bit	0	DISABLE
						1	ENABLE
	1	CH2	RW	0x0	Chanel 2 wait on request enable bit	0	DISABLE
						1	ENABLE
	0	CH1	RW	0x0	Chanel 1 wait on request enable bit	0	DISABLE
						1	ENABLE
DMAINTCTL	0x0024	All	Protect	0x00000000	DMA Interrupt Control Register		
	31:13	Reserved	RO	0x0			
	12	DMA_ERR_INT_EN	RW	0x0	DMA Chanel Error Interrupt Flag Enable	0	DISABLE
						1	ENABLE

	11	DMA_CH4_INT_EN	RW	0x0	DMA Chanel 4 Interrupt Flag Enable	0	DISABLE
						1	ENABLE
	10	DMA_CH3_INT_EN	RW	0x0	DMA Chanel 3 Interrupt Flag Enable	0	DISABLE
						1	ENABLE
	9	DMA_CH2_INT_EN	RW	0x0	DMA Chanel 2 Interrupt Flag Enable	0	DISABLE
						1	ENABLE
	8	DMA_CH1_INT_EN	RW	0x0	DMA Chanel 1 Interrupt Flag Enable	0	DISABLE
						1	ENABLE
	7:5	Reserved	RO	0x0			
	4	DMA_ERR_INT	W1C	0x0	DMA Error Interrupt Flag, Write 1 Clear.		
	3	DMA_CH4_INT	W1C	0x0	DMA Chanel 4 Interrupt Flag, Write 1 Clear.		
	2	DMA_CH3_INT	W1C	0x0	DMA Chanel 3 Interrupt Flag, Write 1 Clear.		
	1	DMA_CH2_INT	W1C	0x0	DMA Chanel 2 Interrupt Flag, Write 1 Clear.		
	0	DMA_CH1_INT	W1C	0x0	DMA Chanel 1 Interrupt Flag, Write 1 Clear.		
UNLOCK	0x0100	All		0x00000055	Unlock Protected Register		
	31:9	Reserved	RO	0x0			
	8	STATUS	RO	0x0	Unlock Status Register	0	LOCK
						1	UNLOCK
	7:0	VAL	RW	0x55	Unlock Value	(x)	(x)

7.20 General Purpose Input/Output (GPIO)

The FP5600 has up to 38 GPIO pins. Depending on the chip configuration, these pins can be shared for multifunction. The 38 pins are arranged in 3 ports called PA, PB and PC. Each of the 38 pins is independent and has a corresponding register bit to control the pin mode function and data.

As shown in Figure 7-16, the I/O type of each I/O pin can be individually configured by firmware as input, output, analog or multifunction mode. For input mode, Schmitt trigger is selectable. For output mode, driving strength is adjustable. After chip reset, the I/O mode of all pins depends on GPIOx->CFG_Pn register.

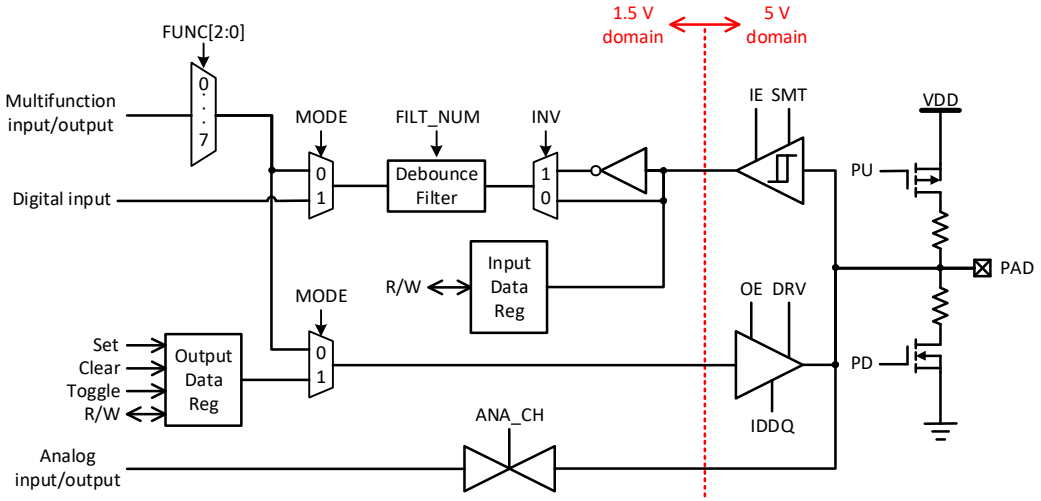


Figure 7-16 GPIO block diagram

7.20.1 GPIO Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
CFG_P0	0x0000	ALL		0x00000000	GPIO Configure Register		
	31:24	FILT_NUM	RW	0x0	Debounce Filter Width (8-bit)	(x)	ADD_ONE_(x)
	23	FILT_SRC	RW	0x0	Debounce Filter Source	0	FROM_FCLK
						1	FROM_LIRC
	22	INV	RW	0x0	Input Inverter Control Bit	0	DISABLE
						1	ENABLE
	21:20	Reserved	RO	0x0			
	19	IE	RW	0x0	Input Enable Bit	0	DISABLE_INPUT
						1	ENABLE_INPUT
	18	SMT	RW	0x0	To switch normal/Schmitt input	0	NORMAL_TRIGGER
						1	SCHMITT_TRIGGER
	17	Reserved	RO	0x0			
	16	OE	RW	0x0	Output Enable Bit	0	DISABLE_OUTPUT
						1	ENABLE_OUTPUT
	15:14	DRV	RW	0x0	Control Driving Strengths	0	DRIVING_STRENGTH_1
						1	DRIVING_STRENGTH_2
						2	DRIVING_STRENGTH_3
						3	DRIVING_STRENGTH_4
	13:10	Reserved	RO	0x0			
	9:8	PUPD	RW	0x0	Pull Up/Down Control bit. Note: This bit is useless when pin as analog function.	0	NO_PULL
						1	PULL_DOWN
						2	PULL_UP
						3	KEEPER
	7	Reserved	RO	0x0			
	6	MODE	RW	0x0	GPIO Mode Selection	0	MULTIFUNCTION
						1	GPIO
	5	Reserved	RO	0x0			
	4	ANA_CH	RW	0x0	Analog Channel Enable Bit	0	DISABLE_ANALOG_CHANNEL
						1	ENABLE_ANALOG_CHANNEL
	3	Reserved	RO	0x0			
	2:0	FUNC	RW	0x0	Multifunction selection bit	0	MULTIFUNCTION_0
						1	MULTIFUNCTION_1
						2	MULTIFUNCTION_2
						3	MULTIFUNCTION_3
						4	MULTIFUNCTION_4
						5	MULTIFUNCTION_5
						6	MULTIFUNCTION_6
						7	MULTIFUNCTION_7
CFG_P1	0x0004	ALL		0x00000000	GPIO Configure Register		
CFG_P2	0x0008	ALL		0x00000000	GPIO Configure Register		
CFG_P3	0x000C	ALL		0x00000000	GPIO Configure Register		
CFG_P4	0x0010	ALL		0x00000000	GPIO Configure Register		
CFG_P5	0x0014	ALL		0x00000000	GPIO Configure Register		
CFG_P6	0x0018	ALL		0x00000000	GPIO Configure Register		
CFG_P7	0x001C	ALL		0x00000000	GPIO Configure Register		
CFG_P8	0x0020	ALL		0x00000000	GPIO Configure Register		
CFG_P9	0x0024	ALL		0x00000000	GPIO Configure Register		
CFG_P10	0x0028	ALL		0x00000000	GPIO Configure Register		
CFG_P11	0x002C	ALL		0x00000000	GPIO Configure Register		
CFG_P12	0x0030	ALL		0x00000000	GPIO Configure Register		
CFG_P13	0x0034	ALL		0x00000000	GPIO Configure Register		
CFG_P14	0x0038	ALL		0x00000000	GPIO Configure Register		
CFG_P15	0x003C	ALL		0x00000000	GPIO Configure Register		
PIN	0x0040	ALL		0x00000000	Reflect Now Pin Value		

	31:16	Reserved	RO	0x0			
	15:0	PIN	RO	0x0	GPIO PAD Level	0	LEVEL_IS_LOW
						1	LEVEL_IS_HIGH
OUT	0x0044	ALL		0x00000000	Pin Output Level Control Register		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	Control corresponding GPIO pad level as bit X(GPIO_AX)	0	OUTPUT_SET_LOW
						1	OUTPUT_SET_HIGH
OUTSET	0x0048	ALL		0x00000000	Set Output Pin Level as High		
	31:16	Reserved	RO	0x0			
	15:0	PIN	WO	0x0	One time set output level	0	NO_EFFECT
						1	OUTPUT_SET_HIGH
OUTCLR	0x004C	ALL		0x00000000	Clear Output Pin Level as Low		
	31:16	Reserved	RO	0x0			
	15:0	PIN	WO	0x0	One time clear output level	0	NO_EFFECT
						1	OUTPUT_SET_LOW
OUTTOGGLE	0x0050	ALL		0x00000000	Toggle Output Pin Level as Low		
	31:16	Reserved	RO	0x0			
	15:0	PIN	WO	0x0	One time toggle output level	0	NO_EFFECT
						1	OUTPUT_TOGGLE
INTMASK	0x0054	ALL		0x00000000	GPIO Interrupt Mask Register		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	Low active register. Disable interrupt occur.	0	CLEAR_INTERRUPT_MASK
						1	SET_INTERRUPT_MASK
INTTYPE	0x0058	ALL		0x00000000	Select Interrupt Type		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	It can be level trigger or edge trigger.	0	LEVEL_TRIGGER
						1	EDGE_TRIGGER
INTBOTH	0x005C	ALL		0x00000000	Both Edge Trigger		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	Select interrupt is single edge or both edge	0	AS_SINGLE_EDGE
						1	BOTH_EDGE
INTPOL	0x0060	ALL		0x00000000	Interrupt Polarity Control		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	Interrupt occurs when High/Low level when level trigger. Interrupt occurs when Rising/Falling level when edge trigger.	0	LOW_OR_FALLING_EDGE
						1	HIGH_OR_RISING_EDGE
INTFLG	0x0064	ALL		0x00000000	GPIO interrupt Flag Register(Latched)		
	31:16	Reserved	RO	0x0			
	15:0	PIN	RW	0x0	GPIO Pin x Interrupt	0	NOT_OCCUR
						1	OCCUR\WRITE_1_CLEAR

7.21 Coordinate Rotation Digital Computer (CORDIC)

The CORDIC algorithm is a useful convergent method for the calculation of trigonometric, linear, and related functions. The algorithm can perform not only vector rotations in the Euclidean plane, but also mass rotations in the linear plane.

The CORDIC algorithm is an iterative process, and truncation error is an inherent property of this process.

The CORDIC coprocessor uses up to 31 iterations per calculation and uses a core data width of at least 32 bits, resulting in high precision. The main advantage of using this algorithm is that it has faster calculation speed than software and can obtain high accuracy.

Machine Mode \ Transform Type	Rotation Mode	Vector Mode
Circular Type	$X \rightarrow CORDIC \rightarrow K(X\cos W - Y\sin W)$ $Y \rightarrow CORDIC \rightarrow K(Y\cos W + X\sin W)$ $W \rightarrow CORDIC \rightarrow 0$	$X \rightarrow CORDIC \rightarrow K\sqrt{X^2 + Y^2}$ $Y \rightarrow CORDIC \rightarrow 0$ $W \rightarrow CORDIC \rightarrow W + \tan^{-1}\frac{Y}{X}$
Linear Type	$X \rightarrow CORDIC \rightarrow X$ $Y \rightarrow CORDIC \rightarrow Y + X \cdot W$ $W \rightarrow CORDIC \rightarrow 0$	$X \rightarrow CORDIC \rightarrow X$ $Y \rightarrow CORDIC \rightarrow 0$ $W \rightarrow CORDIC \rightarrow W + \frac{Y}{X}$

Table 7-1 CORDIC Machine Mode and Transform Type

7.21.1 CORDIC Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
X_IN	0x0000	ALL		0x00000000	CORDIC X element input register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)
Y_IN	0x0004	ALL		0x00000000	CORDIC Y element input register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)
W_IN	0x0008	ALL		0x00000000	CORDIC W element input register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)
COCTL	0x000C	ALL		0x00000000	CORDIC Control Register		
	31:20	Reserved	RO	0x0			
	24	OVF	W1C	0x0	Overflow flag.	0	NO_EFFECT
						1	OCCUR\WRITE_1_CLEAR
	23:20	Reserved	RO	0x0			
	19	RESCALE	RW	0x0	Enable hardware auto scale the final result of X and Y by different transform.	0	DISABLE
						1	ENABLE
	18	MODE	RW	0x0	Machine mode selection	0	VECTOR
						1	ROTATION
	17:16	TRANS	RW	0x0	Transform type selection	0	CIRCULAR
						1	LINEAR
						2	HYPERBOLIC
						3	Reserved
	15:13	Reserved	RO	0x0	Reserved		
	12:8	ITERA_TIMES	RW	0x0	CORDIC iteration times configuration. (5 bit)	(x)	(x)
	7:2	Reserved	RO	0x0	Reserved		
	1	RST_EN	W1S	0x0	Reset CORDIC engine and stop.	0	NO_EFFECT
						1	ENABLE
	0	RUN	W1S	0x0	Enable CORDIC calculation by control register set.	0	NO_EFFECT
						1	ENABLE
X_OUT	0x0010	ALL		0x00000000	CORDIC X element output register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)
Y_OUT	0x0014	ALL		0x00000000	CORDIC Y element output register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)

W_OUT	0x0018	ALL		0x00000000	CORDIC W element output register		
	31:0	VAL	RW	0x0	32 bit register	(x)	(x)

7.21.2 HDIV Register Map

Register Name	Bit Index	Field Name	Access	Default	Description	Option	FW Label
DIVIDEND	0x0000	ALL		0x00000000	Dividend of hardware divider		
	31:0	VAL	RW	0x0	32 bit signed register	(x)	(x)
DIVISOR	0x0004	ALL		0x00000000	Divisor of hardware divider		
	31:0	VAL	RW	0x0	32 bit signed register	(x)	(x)
DIVSTS	0x0008	ALL		0x00000000	Divider Status Register		
	31:1	Reserved	RO	0x0			
	0	DIVZERO	RO	0x0	When dividend is zero, this bit is set and cleared by hardware after calculation. Whenever DIVISOR is written, this bit will be '0' when DIVISOR is non-zero and becomes '1' when divisor=0.	0	NOT_OCCUR
						1	OCCUR
QUO	0x000C	ALL		0x00000000	Quotient Result Register		
	31:0	VAL	RW	0x0	32 bit signed register	(x)	(x)
REM	0x0010	ALL		0x00000000	Remainder Result Register		
	31:0	VAL	RW	0x0	32 bit signed register	(x)	(x)