RICOH

R3200x SERIES

RESET TIMER IC FOR MOBILE EQUIPMENTS

NO.EA-280-110705

OUTLINE

The R3200x Series are reset timer ICs with two input signals for mobile equipments which require long interval for reset sequence. The long interval prevents unexpected resets caused by accidental key operations. Internally, each of these ICs consist of a delay generator circuit and output driver transistors.

The R3200x Series have two active-low input pins ($\overline{SR0}$ and $\overline{SR1}$) which generate reset signals after output delay time when both input pins are activated at the same time. The output delay time of the reset signals is user-selectable options of 7.5s or 11.25s by connecting DSR to either GND or V_{DD}.

While the reset signals are remaining active or being sent out, the ICs provide ultra-low supply current.

The R3200x Series are available in DFN(PLP)2020-8B and DFN1216-8 (Under Development) packages.

FEATURES

- Supply Current 1 (at standby) ..... Typ. 0.28μA (V_{DD}=5.5V)
- Supply Current 2 (at active before reset signal output) ..... Typ. 3μA (V_{DD}=5.5V) *
- Supply Current 3 (at active after reset signal output) ..... Typ. 0.45μA (V_{DD}=5.5V)
- Operating Voltage Range ..... 1.65V to 5.5V
- Operating Temperature Range ..... −40 to 85 °C
- Output Delay Time ..... Typ. 7.5s or 11.25s Selectable
- Output Delay Time Accuracy ..... ±20%
- Output Types ..... Nch Open Drain and CMOS
- Packages ..... DFN(PLP)2020-8B, DFN1216-8 (Under Development)

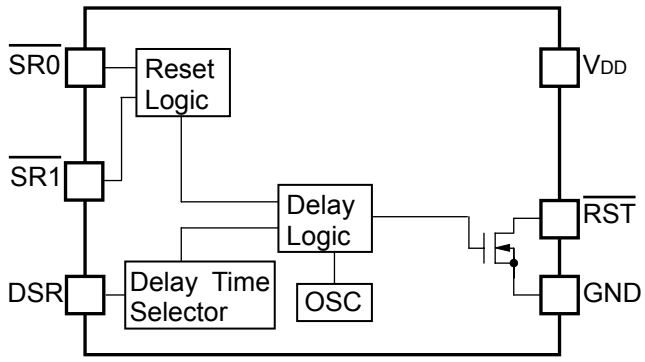
*) Guaranteed by design engineering.

APPLICATIONS

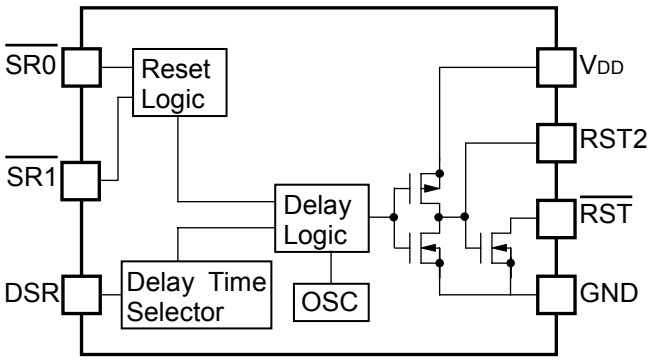
- Mobile phone, Smartphone
- E-book, Tablet devices
- Portable Games
- Personal Navigation Devices

BLOCK DIAGRAMS

R3200x001A



R3200x001B



SELECTION GUIDE

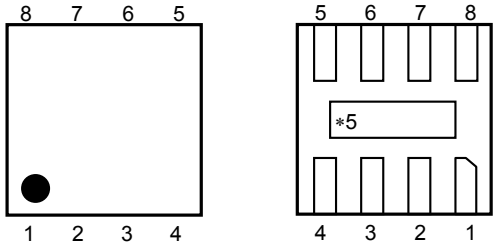
The package type and the output type for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3200K001∗-TR	DFN(PLP)2020-8B	5,000 pcs	Yes	Yes
R3200L001∗-E2	DFN1216-8	5,000 pcs	Yes	Yes

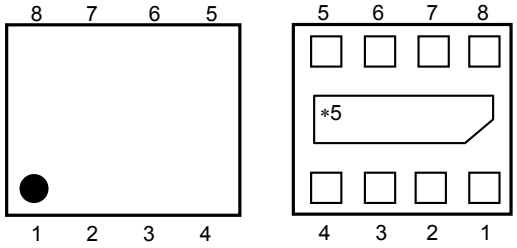
∗ : Designation of Output Type
(A) Nch Open Drain
(B) Nch Open Drain and CMOS

PIN CONFIGURATIONS

● **DFN(PLP)2020-8B**



● **DFN1216-8 (Under Development)**



PIN DESCRIPTIONS

● **DFN(PLP)2020-8B, DFN1216-8 (Under Development)**

Pin No.	Symbol	Description
1	NC	No Connection (Only for A version)
	RST2	CMOS Output Pin, "H" Active (Only for B version)
2	GND	Ground Pin
3	$\overline{SR1}$	2nd Reset Input Pin, ("L" Active) *1
4	$\overline{RST}$	Nch Open Drain Output Pin, ("L" Active) *2
5	DSR	Output Delay Time Selection Pin (GND: 7.5s, V_{DD}: 11.25s) *3
6	TEST	Test Pin *4
7	$\overline{SR0}$	1st Reset Input Pin, ("L" Active) *1
8	V_{DD}	Power Supply Input Pin

∗1) In the case of using one "L" active input signal pin, either $\overline{SR0}$ or $\overline{SR1}$ must be connected to GND.
∗2) In the case of using B version without $\overline{RST}$, $\overline{RST}$ must be connected to GND or left open.
∗3) DSR pin must be connected to either GND or V_{DD}.
∗4) TEST must be connected to GND.
∗5) Tab is GND level. (They are connected to the reverse side of this IC.)
The tab is better to be connected to the GND, but leaving it open is also acceptable.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply Voltage	GND-0.3 to 6.0	V
V_{SR0}	Input Voltage (1st Reset input pin)	GND-0.3 to 6.0	V
V_{SR1}	Input Voltage (2nd Reset input pin)	GND-0.3 to 6.0	V
V_{RST}	Output Voltage (1st Reset output pin)	GND-0.3 to 6.0	V
V_{RST2}	Output Voltage (2nd Reset output pin)	GND-0.3 to V_{DD}+0.3	V
V_{DSR}	Input Voltage (Output Delay Time Selection Pin)	GND-0.3 to 6.0	V
I_{OUT}	Output Current	20	mA
P_D	Power Dissipation (DFN(PLP)2020-8B)*	880	mW
	Power Dissipation (DFN1216-8)* (Under Development)	625	
Topt	Operating Temperature Range	−40 to 85	°C
Tstg	Storage Temperature Range	−55 to 125	°C

∗) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

- **R3200x**

The specification in ☐ is checked and guaranteed by design engineering at –40°C ≤ T_{opt} ≤ 85°C.

Topt=25°C

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			1.65		5.5	V
I_{SS1}	Supply Current1	V_{DD}=5.5V, at standby			0.28	1.35	µA
I_{SS2}	Supply Current2	V_{DD}=5.5V, at active before reset signal output			3.0	6.5	µA
I_{SS3}	Supply Current3	V_{DD}=5.5V, at active after reset signal output			0.45	1.7	µA
V_{OL}	"L" Output Voltage	V_{DD} ≥ 4.5V	I_{OL}=8mA			0.3	V
		V_{DD} ≥ 3.3V	I_{OL}=5mA				
		V_{DD} ≥ 1.65V	I_{OL}=3mA				
V_{OH}	"H" Output Voltage (Only for B version)	V_{DD} ≥ 4.5V	I_{OH}=5mA	V_{DD} x 0.85			V
		V_{DD} ≥ 3.3V	I_{OH}=2.5mA				
		V_{DD} ≥ 1.65V	I_{OH}=0.8mA				
I_{LEAKI}	$\overline{SR0}$, $\overline{SR1}$ Input Leakage Current	V_{DD} = 5.5V				0.1	µA
I_{LEAKO}	Output Leakage Current	V_{DD} = 5.5V				0.1	µA
t_{DELAY}	Output Delay Time	DSR=GND		6	7.5	9	s
		DSR=V_{DD}		9	11.25	13.5	s
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltaget					0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltaget			0.85			V

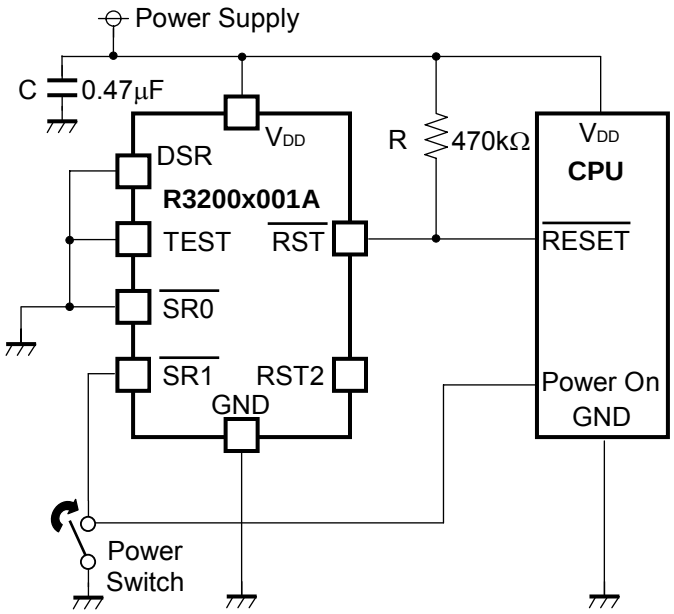
All of units are tested and specified under load conditions such that Tj≈Topt=25°C except for Supply Current2.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

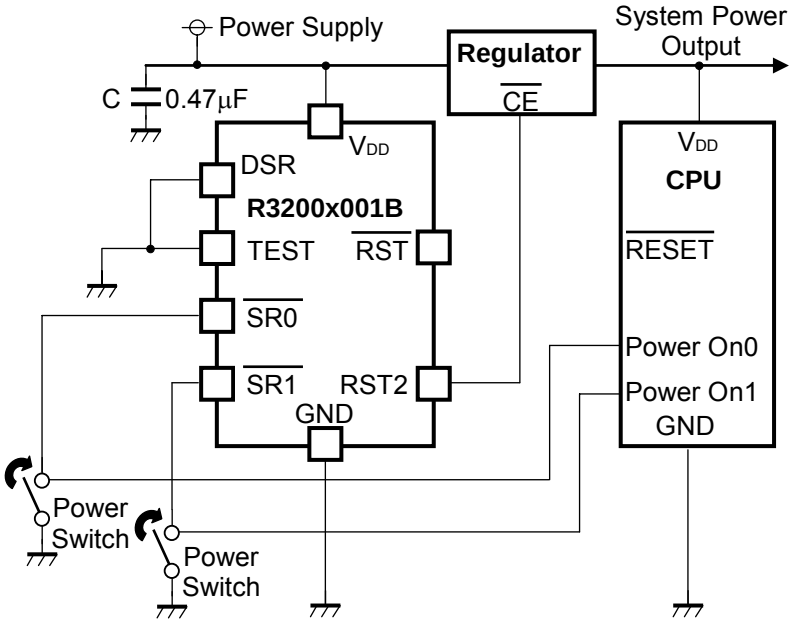
TYPICAL APPLICATIONS

- **R3200x001A**



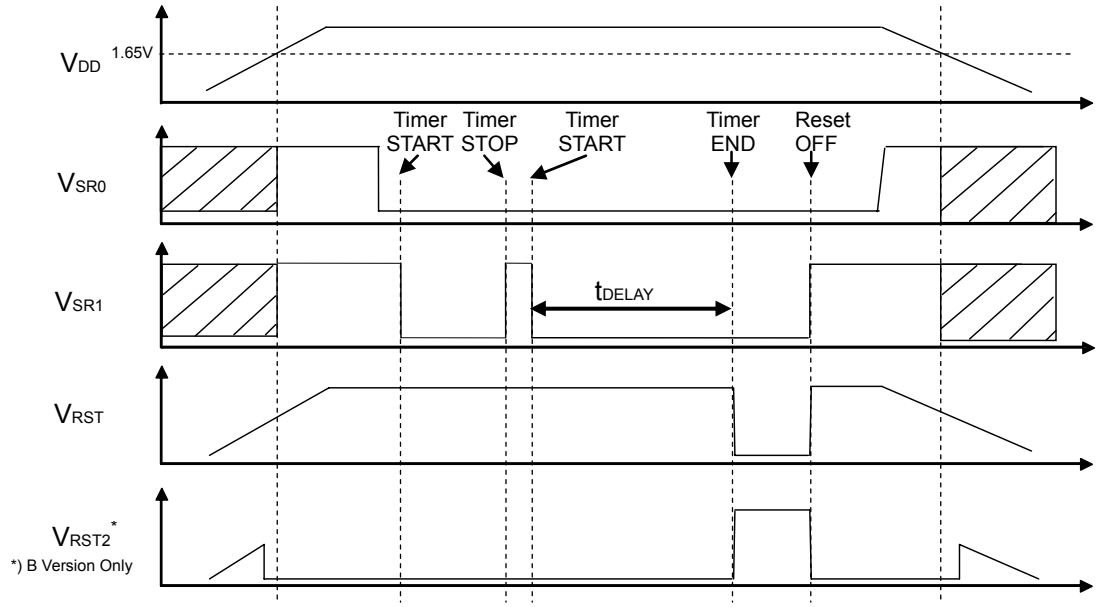
$\overline{\text{RST}}$ pin should be pulled up with a resistor. The recommended value for the resistor is 470kΩ.
In the case of using one active-low input signal-pin, either $\overline{\text{SR0}}$ or $\overline{\text{SR1}}$ pin should be connected to GND.

- **R3200x001B**



(External Components)
C: Ceramic 0.47μF Ex. Murata GRM155B30J474KE18

TIMING CHART



OPERATION

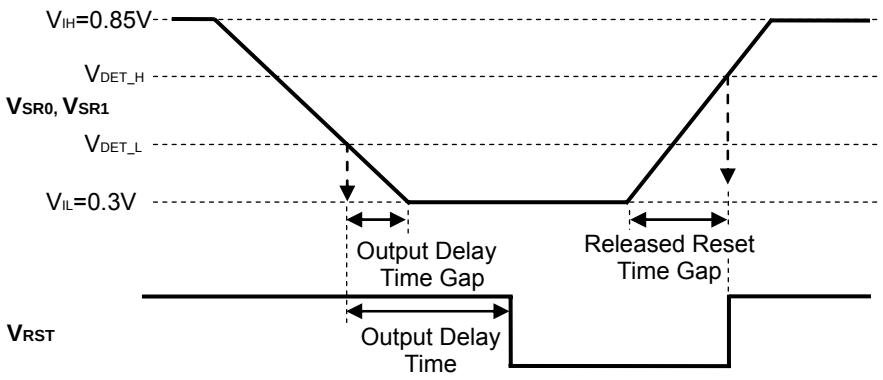
When both $\overline{SR0}$ and $\overline{SR1}$ voltages become lower than V_{IL}, the timer operation will be start. And then, after t_{DELAY}, "reset" will be generated.

If either SR0 or SR1 voltage become higher than V_{IL}, the timer operation will not start.

During the output delay time, if either $\overline{SR0}$ or $\overline{SR1}$ becomes higher than the V_{IH}, the timer operation will stop. Again If both $\overline{SR0}$ and $\overline{SR1}$ voltages become lower than V_{IL} again after t_{DELAY}, the "reset" will be generated. While the reset signal is being sent, either $\overline{SR0}$ or $\overline{SR1}$ voltage becomes higher than V_{IH}, the reset signal will be canceled. Until either $\overline{SR0}$ or $\overline{SR1}$ voltage becomes higher than V_{IH}, the reset signal will be continually sent out.

OUTPUT DELAY TIME GAP

The threshold voltages of $\overline{SR0}$ and $\overline{SR1}$ are between V_{IL} and V_{IH}. Therefore, if the rising or falling slew rate is very slow, the timer will start at the point of crossing the threshold voltage and may cause errors in the output delay time (t_{DELAY}) and the released reset time.



Example: Relation between the Rising and Falling Slew Rate and the Time Gap

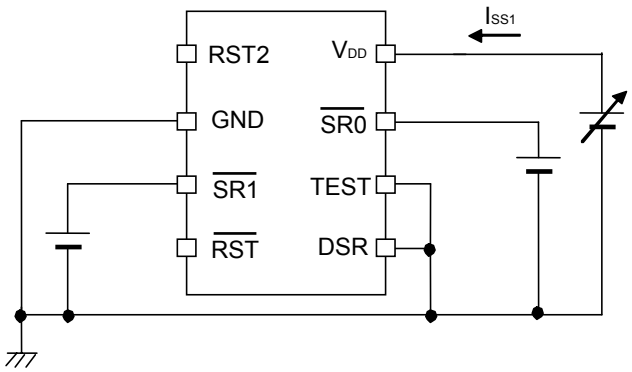
OUTPUT DELAY TIME SWITCHING

The output delay time can be selected 7.5s (Typ.) or 11.25s (Typ.) by connecting DSR to either GND or to V_{DD}. However, if DSR is switched during the operations, the output would become unstable and may cause false operations. Switching DSR must be done during power-off. Also, DSR must be connected to either GND or V_{DD} because if DSR pin is not connected to either GND or V_{DD}, the output would become unstable and may cause false operations.

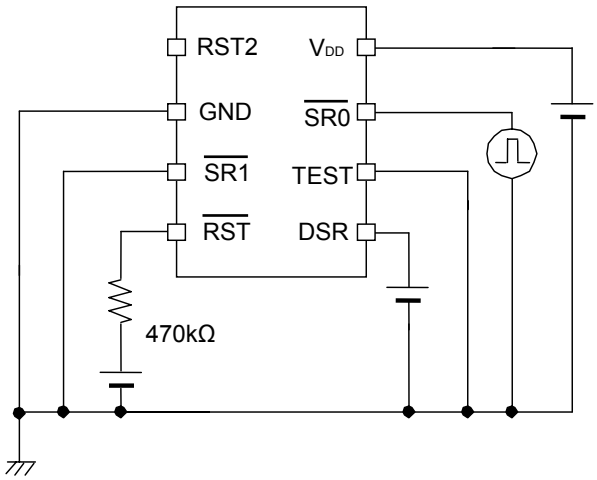
PRECAUTIONS: V_{DD} Start-up during Low Input

When starting up V_{DD} at slow slew rate of 0.001V/µs or less with the low $\overline{SR0}$ and $\overline{SR1}$ voltages, the ICs may start the operation at lower than the minimum operating voltage, thus the output delay time may exceed the guaranteed time.

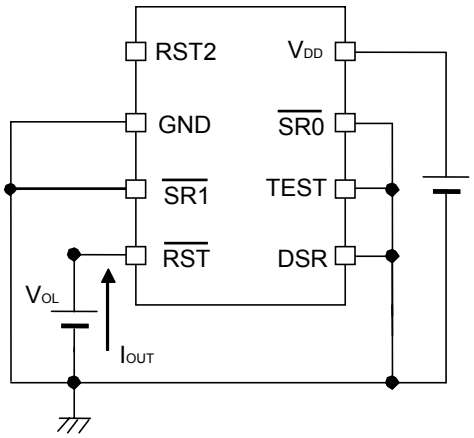
TEST CIRCUITS



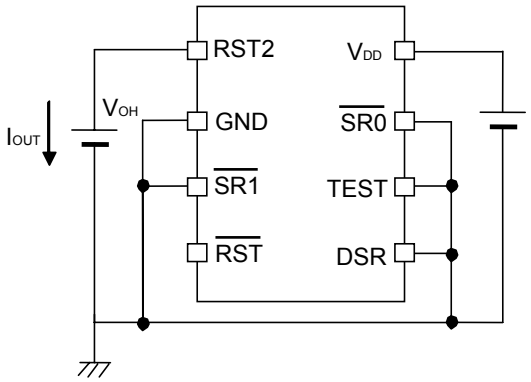
Supply Current Test Circuit



Output Delay Time Test Circuit



NMOS Driver Output Voltage Test Circuit



CMOS Driver Output Voltage Test Circuit (B version only)

PRECAUTIONS: Circuit Configuration

In the case of applying the following circuit configuration (Fig.A) to the R3200x001A/B Series, if the R1 value is high, the ICs own supply current may cause significant voltage drop to V_{DD} pin, and V_{DD} voltage may fall below the minimum operating voltage.

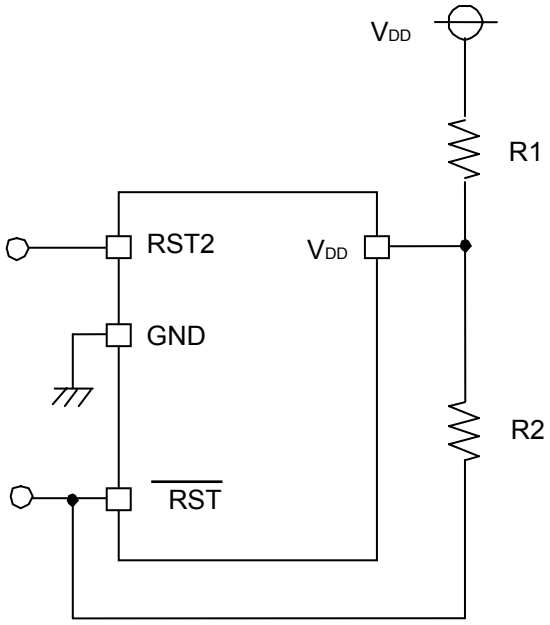
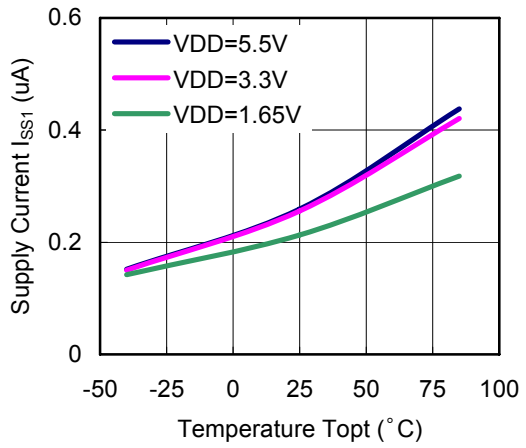


Fig. A

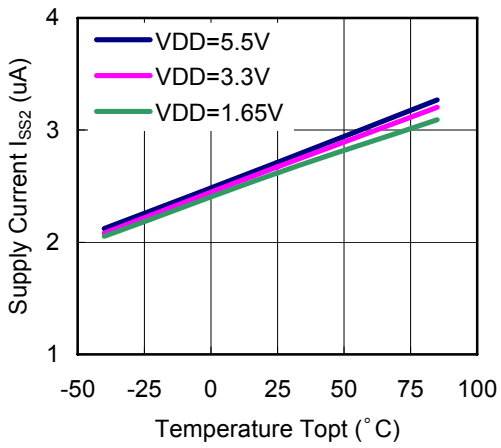
TYPICAL CHARACTERISTICS

1) Supply Current vs. Temperature

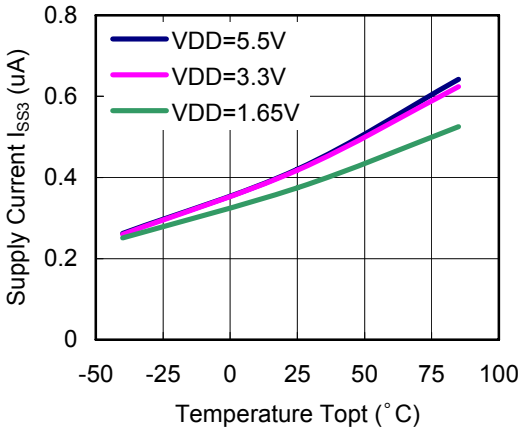
Supply Current1 (I_{SS1}) (at standby)



Supply Current2 (I_{SS2}) (at active before the reset signal output)

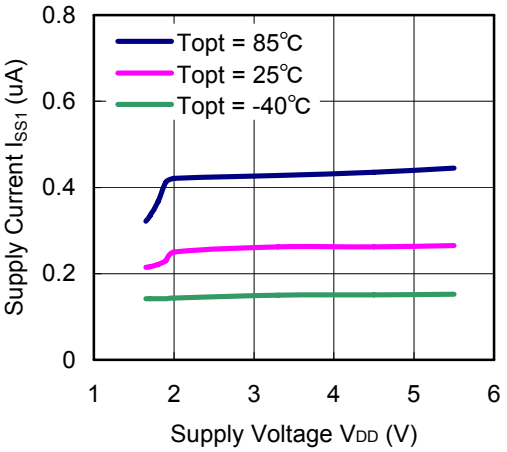


Supply Current3 (I_{SS3}) (at active after the reset signal output)

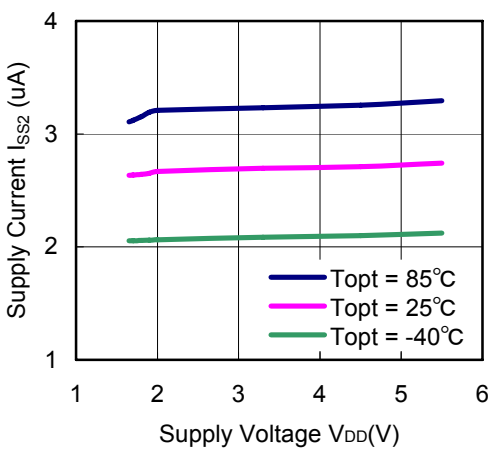


2) Supply Current vs. Supply Voltage

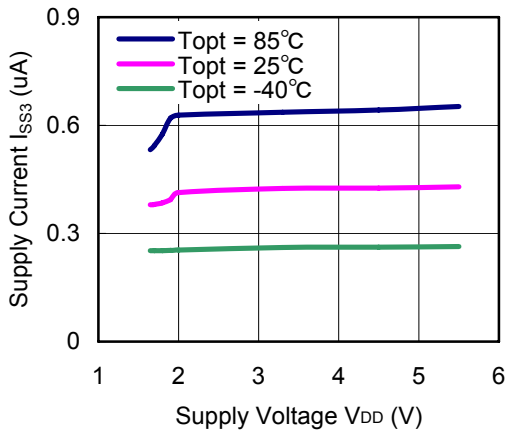
Supply Current1 (I_{SS1})



Supply Current2 (I_{SS2})

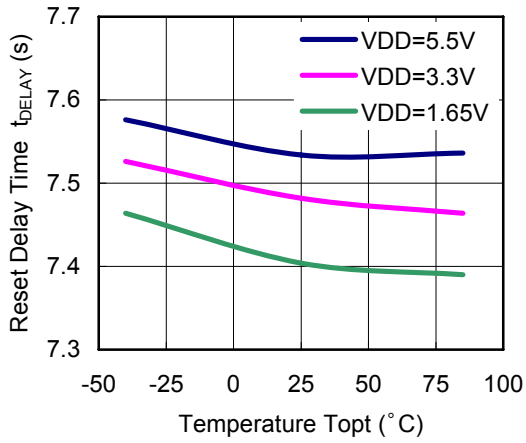


Supply Current3 (I_{SS3})

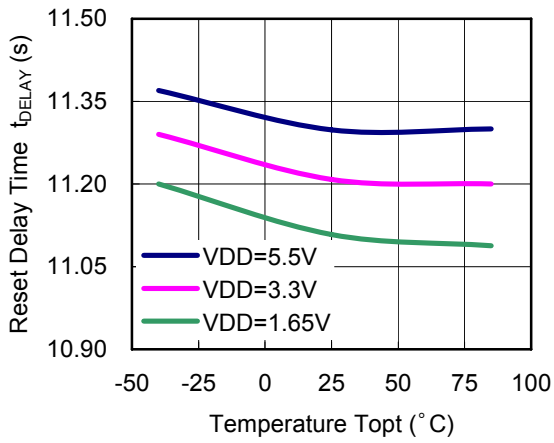


3) Output Delay Time vs. Temperature

DSR = GND (Typ. 7.5s)

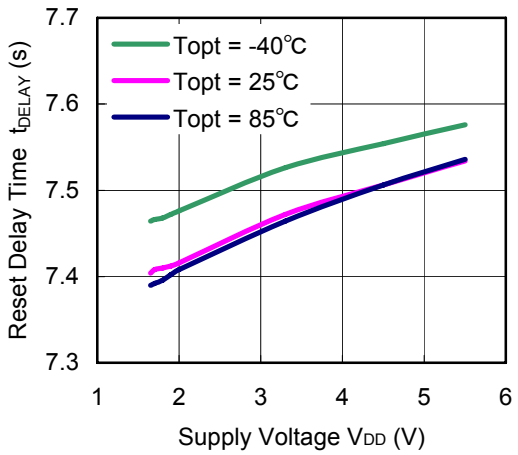


DSR = V_{DD} (Typ. 11.25s)

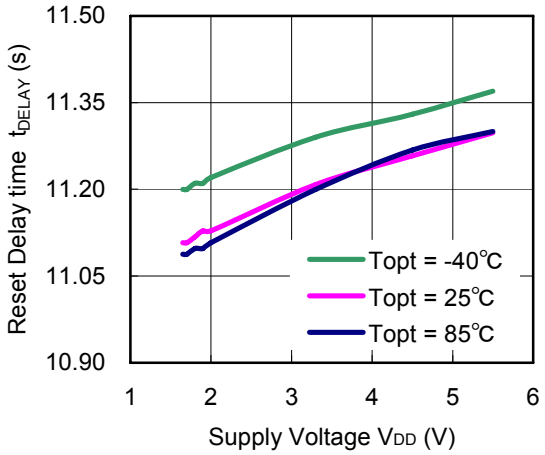


4) Output Delay Time vs. Supply Voltage

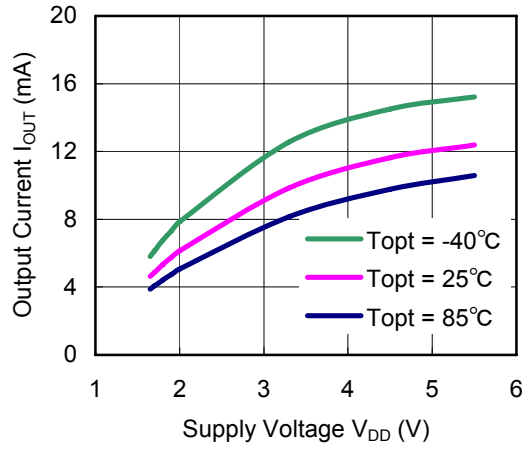
DSR = GND (Typ. 7.5s)



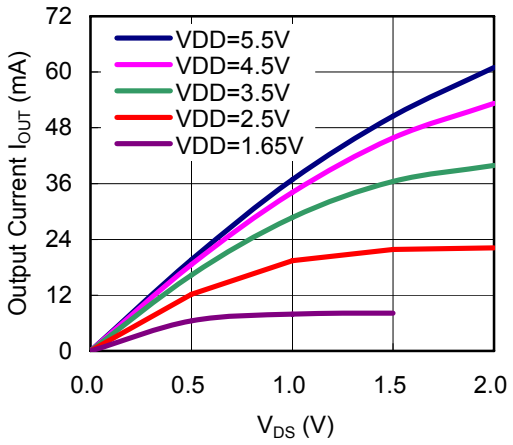
DSR = V_{DD} (Typ. 11.25s)



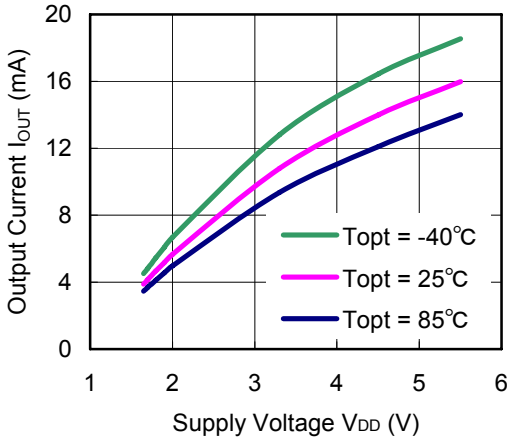
5) Nch Driver Output Current vs. Supply Voltage
V_{DS}=0.3V



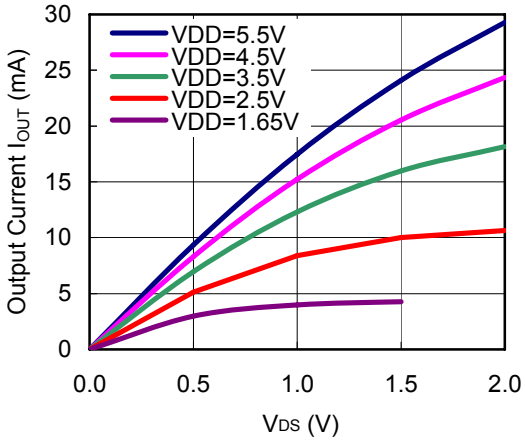
6) Nch Driver Output Current vs. V_{DS}



7) Pch Driver Output Current vs. Supply Voltage
V_{DS}=0.9V



8) Pch Driver Output Current vs. V_{DS}



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