

## LOW VOLTAGE DETECTOR with individual SENSE pin and delay function

NO.EA-242-100929

### OUTLINE

The R3118x series are CMOS-based voltage detector ICs with individual sense pin, high detector threshold accuracy and delay time, and ultra-low supply current, which can be operated at an extremely low voltage and is used for system reset as an example.

Each of these ICs consists of a voltage reference unit, a hysteresis comparator, resistors net for detector threshold setting, an output driver transistor, and a delay circuit.

$V_{DD}$  supply pin for the IC and voltage supervisory sense pin are individual, therefore the output pin can keep "L" level even if the sense pin voltage is going down to 0V, or there is no indefinite range for the sense pin.

Since a delay circuit is built-in, by connecting an external capacitor, any output delay time can be set. In the R3118x series, detector released delay time can be set, and detector delay time is not influenced by the external capacitor for the delay time.

The detector threshold is fixed with high accuracy internally and does not require any adjustment.

The tolerance of the detector threshold is  $\pm 22.5\text{mV}$  ( $-V_{DET\_S} < 1.6\text{V}$ ) or  $\pm 1.5\%$  ( $-V_{DET\_S} \geq 1.6\text{V}$ ).

Minimum detector threshold voltage is 0.6V, ultra low voltage detector threshold can be set.

Output delay time for the detector release can be set with high accuracy. The tolerance of the IC side is  $\pm 30\%$ .

Two output types, Nch open drain type and CMOS type are available. If the sense pin voltage becomes to equal or lower than the detector threshold voltage, the output voltage becomes "L", and if the sense pin voltage becomes to released voltage, the output voltage becomes "H" after the set delay time.

Three types of packages, SOT-23-5, SC-88A, and DFN(PLP)1212-6 are available.

### FEATURES\*

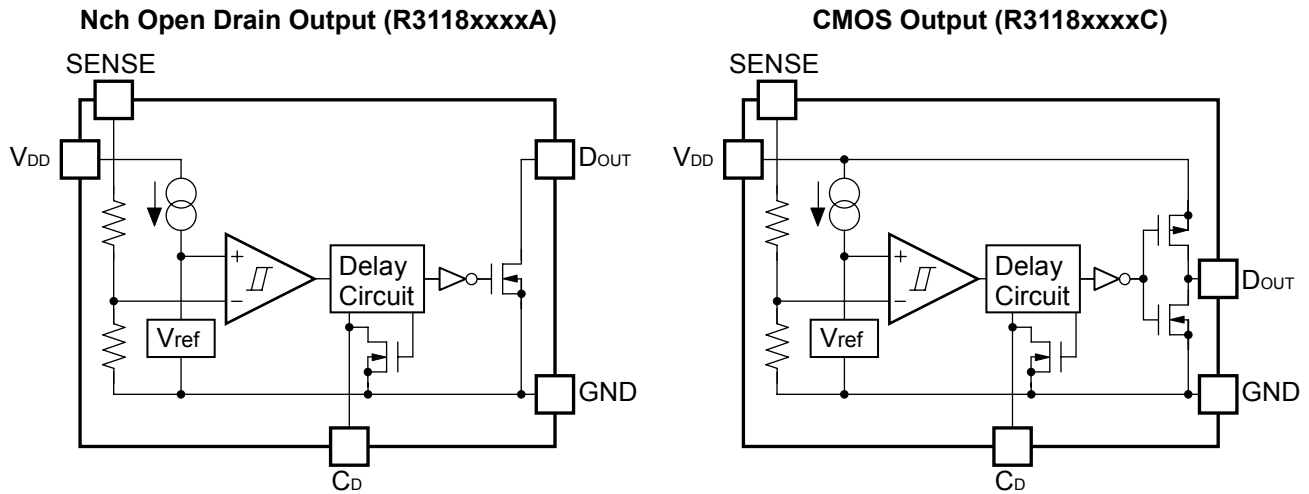
- Supply Current ..... Typ. 0.4 $\mu\text{A}$  ( $V_{SENSE} \geq +V_{DET}$ ,  $V_{DD}=6\text{V}$ )  
Consumption current through SENSE pin is not included.
- Operating Voltage Range ..... 1.0V to 6.0V ( $-40^\circ\text{C} \leq T_{opt} \leq 85^\circ\text{C}$ )
- Detector Threshold Range ..... 0.6V to 5.0V (0.1V steps)  
(For other voltages, please refer to MARK INFORMATIONS.)
- Accuracy Detector Threshold .....  $\pm 1.5\%$  ( $-V_{DET\_S} \geq 1.6\text{V}$ ),  $\pm 22.5\text{mV}$  ( $-V_{DET\_S} < 1.6\text{V}$ )
- Temperature-Drift Coefficient of Detector Threshold ..... Typ.  $\pm 30\text{ppm}/^\circ\text{C}$
- Accuracy Detector Released .....  $\pm 30\%$
- Temperature-Drift Coefficient of Detector Released ..... Typ.  $\pm 0.16\text{ppm}/^\circ\text{C}$
- Output Types ..... Nch Open Drain and CMOS
- Packages ..... DFN(PLP)1212-6, SC-88A, SOT-23-5

\*  $T_{opt}=25^\circ\text{C}$ , unless otherwise noted.

### APPLICATIONS

- CPU and Logic Circuit Reset
- Battery Checker
- Window Comparator / Level discrimination
- Battery Back-up Circuit
- Power Failure Detector

## BLOCK DIAGRAMS



## SELECTION GUIDE

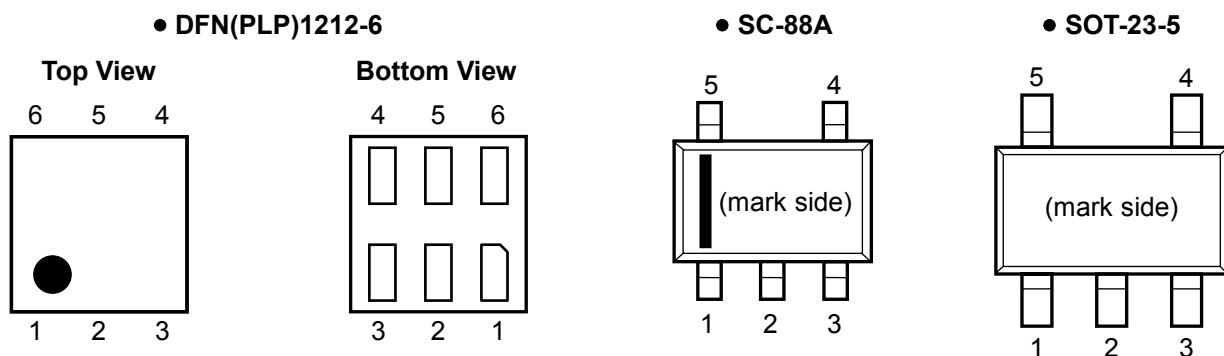
The package type, the detector threshold, the output type and the taping type for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3118Kxx1*-TR	DFN(PLP)1212-6	5,000 pcs	Yes	Yes
R3118Qxx2*-TR-FE	SC-88A	3,000 pcs	Yes	Yes
R3118Nxx1*-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

xx: The detector threshold can be designated in the range from 0.6V(06) to 5.0V(50) in 0.1V steps.  
(For other voltages, please refer to MARK INFORMATIONS.)

\* : Designation of Output Type  
(A) Nch Open Drain  
(C) CMOS

## PIN CONFIGURATIONS



## PIN DESCRIPTIONS

### • DFN(PLP)1212-6

Pin No.	Symbol	Description
1	SENSE	Voltage Detector Voltage Sense Pin
2	GND	Ground Pin
3	C <sub>D</sub>	Pin for External Capacitor (for setting output delay)
4	V <sub>DD</sub>	Input Pin
5	NC	No Connection
6	D <sub>OUT</sub>	Output Pin ("L" at detection, "H" at released)

### • SC-88A

Pin No.	Symbol	Description
1	D <sub>OUT</sub>	Output Pin ("L" at detection, "H" at released)
2	GND	Ground Pin
3	V <sub>DD</sub>	Input Pin
4	C <sub>D</sub>	Pin for External Capacitor (for setting output delay)
5	SENSE	Voltage Detector Voltage Sense Pin

### • SOT-23-5

Pin No.	Symbol	Description
1	D <sub>OUT</sub>	Output Pin ("L" at detection, "H" at released)
2	V <sub>DD</sub>	Input Pin
3	GND	Ground Pin
4	C <sub>D</sub>	Pin for External Capacitor (for setting output delay)
5	SENSE	Voltage Detector Voltage Sense Pin

## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V <sub>DD</sub>	Supply Voltage	-0.3 to 7.0	V
V <sub>SENSE</sub>	SENSE Pin Voltage	-0.3 to 7.0	V
V <sub>DOUT</sub>	Output Voltage (Nch Open Drain Output)	-0.3 to 7.0	V
	Output Voltage (CMOS Output)	-0.3 to V <sub>DD</sub> +0.3	
I <sub>DOUT</sub>	Output Current Nch Driver (Sink Current)	20	mA
	Output Current Pch Driver (Source Current)	-5	
P <sub>D</sub>	Power Dissipation (DFN(PLP)1212-6) *	400	mW
	Power Dissipation (SC-88A)*	380	
	Power Dissipation (SOT-23-5) *	420	
T <sub>opt</sub>	Operating Temperature Range	-40 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 125	°C

\* ) For Power Dissipation, please refer to PACKAGE INFORMATION.

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

## ELECTRICAL CHARACTERISTICS

### • R3118xxxxA/C

  values indicate  $-40^{\circ}\text{C} \leq T_{\text{opt}} \leq 85^{\circ}\text{C}$ ,  $-V_{\text{DET\_S}}$  means set detector threshold,  $V_{\text{DD}}=1\text{V to }6\text{V}$ , unless otherwise noted.

T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Operating Voltage		1		6	V	
-V <sub>DET</sub>	Detector Threshold	-V <sub>DET_S</sub> < 1.6V	T <sub>opt</sub> =25°C	-V <sub>DET_S</sub> -0.0225	-V <sub>DET_S</sub>	-V <sub>DET_S</sub> +0.0225	V
			-40°C ≤ T <sub>opt</sub> ≤ 85°C	-V <sub>DET_S</sub> -0.0375	-V <sub>DET_S</sub>	-V <sub>DET_S</sub> +0.0375	
		-V <sub>DET_S</sub> ≥ 1.6V	T <sub>opt</sub> =25°C	-V <sub>DET_S</sub> × 0.985	-V <sub>DET_S</sub>	-V <sub>DET_S</sub> × 1.015	
			-40°C ≤ T <sub>opt</sub> ≤ 85°C	-V <sub>DET_S</sub> × 0.975	-V <sub>DET_S</sub>	-V <sub>DET_S</sub> × 1.025	
V <sub>HYS</sub>	Detector threshold Hysteresis	T <sub>opt</sub> =25°C	-V <sub>DET_S</sub> × 0.040	-V <sub>DET_S</sub> × 0.055	-V <sub>DET_S</sub> × 0.070	V	
		-40°C ≤ T <sub>opt</sub> ≤ 85°C	-V <sub>DET_S</sub> × 0.035	-V <sub>DET_S</sub> × 0.055	-V <sub>DET_S</sub> × 0.075		

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I <sub>SS</sub>	Supply Current *1	V <sub>SENSE</sub> =0V, V <sub>DD</sub> =6V		0.480	1.450	μA
		V <sub>SENSE</sub> =6V, V <sub>DD</sub> =6V		0.400	1.200	
R <sub>SENSE</sub>	Sense Resistor	V <sub>SENSE</sub> =6V, V <sub>DD</sub> =6V	9	34	58	MΩ
I <sub>DOUT</sub>	Output Current (Driver Output Pin)	Nch V <sub>SENSE</sub> =0V	V <sub>DD</sub> =1V, V <sub>DOUT</sub> =0.1V	0.150		mA
			V <sub>DD</sub> =3V, V <sub>DOUT</sub> =0.1V	0.550		
			V <sub>DD</sub> =5V, V <sub>DOUT</sub> =0.1V	0.850		
			V <sub>DD</sub> =1V, V <sub>DOUT</sub> =0.4V	0.400		
			V <sub>DD</sub> =3V, V <sub>DOUT</sub> =0.4V	2.100		
			V <sub>DD</sub> =5V, V <sub>DOUT</sub> =0.4V	3.300		
		Pch *2 V <sub>SENSE</sub> =6V	V <sub>DD</sub> =1V, V <sub>DOUT</sub> =0.9V	6		μA
			V <sub>DD</sub> =3V, V <sub>DOUT</sub> =2.9V	30		
			V <sub>DD</sub> =5V, V <sub>DOUT</sub> =4.9V	45		
I <sub>LEAK</sub>	Nch Driver Leakage Current *3	V <sub>SENSE</sub> =6V, V <sub>DD</sub> =6V, V <sub>DOUT</sub> =6V			80	nA
R <sub>DIS</sub>	C <sub>D</sub> pin Discharge Tr. On Resistance	V <sub>SENSE</sub> =6V, V <sub>DD</sub> =1V, V <sub>CD</sub> =0.4V	2.200		6.200	kΩ
		V <sub>SENSE</sub> =6V, V <sub>DD</sub> =3V, V <sub>CD</sub> =0.4V	0.400		1.250	
		V <sub>SENSE</sub> =6V, V <sub>DD</sub> =5V, V <sub>CD</sub> =0.4V	0.250		0.800	
t <sub>reset</sub>	Detect Output Delay Time *4	T <sub>opt</sub> =25°C		80		μs
t <sub>delay</sub>	Release Output Delay Time *5	T <sub>opt</sub> =25°C	70	100	130	ms
		-40°C ≤ T <sub>opt</sub> ≤ 85°C	65	100	145	

All of unit are tested and specified under load conditions such that T<sub>opt</sub>=25°C except for Detector Threshold Temperature Coefficient, Detector Output Delay Time and Release Output Delay Time.

\*1: Consumption current through SENSE pin is not included.

\*2: In case of CMOS type

\*3: In case of Nch Open Drain type

\*4: In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C<sub>D</sub> pin, the time interval from forcing pulsive voltage between -V<sub>DET\_SX</sub>1.155V and -V<sub>DET\_SX</sub>0.9 to SENSE pin, to when the output voltage of the D<sub>OUT</sub> pin will reach from "H" to V<sub>DD</sub>/2.

In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C<sub>D</sub> pin and the D<sub>OUT</sub> pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between -V<sub>DET\_SX</sub>1.155V and -V<sub>DET\_SX</sub>0.9V to SENSE pin, to when the output voltage reaches from "H" to 2.5V.

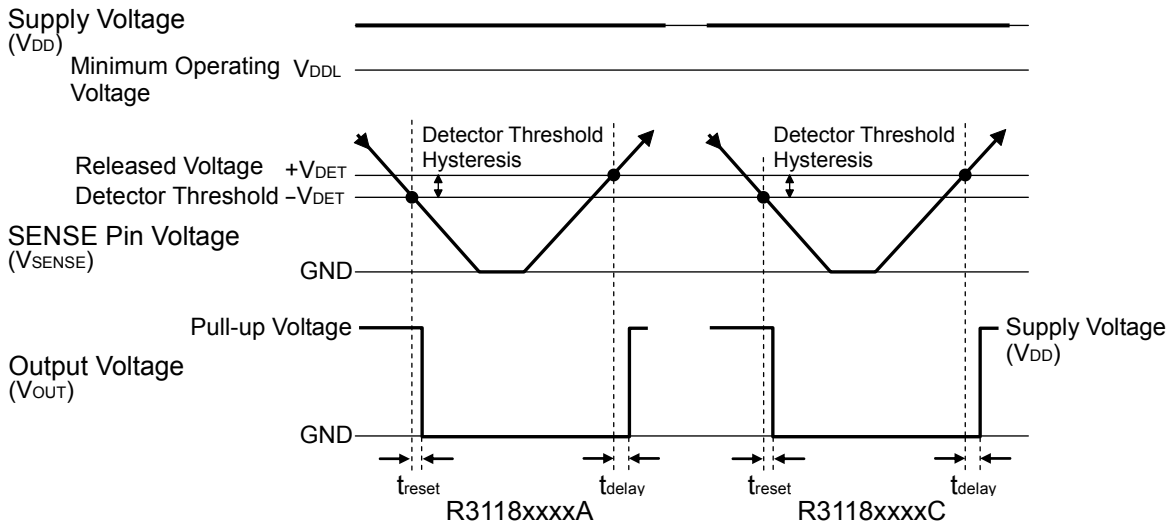
\*5: In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C<sub>D</sub> pin, the time interval from forcing pulsive voltage between -V<sub>DET\_SX</sub>0.9 and -V<sub>DET\_SX</sub>1.155V to SENSE pin, to when the output voltage of the D<sub>OUT</sub> pin will reach from "L" to V<sub>DD</sub>/2.

In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C<sub>D</sub> pin and the D<sub>OUT</sub> pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between -V<sub>DET\_SX</sub>0.9V and -V<sub>DET\_SX</sub>1.155V to SENSE pin, to when the output voltage reaches from "L" to 2.5V.

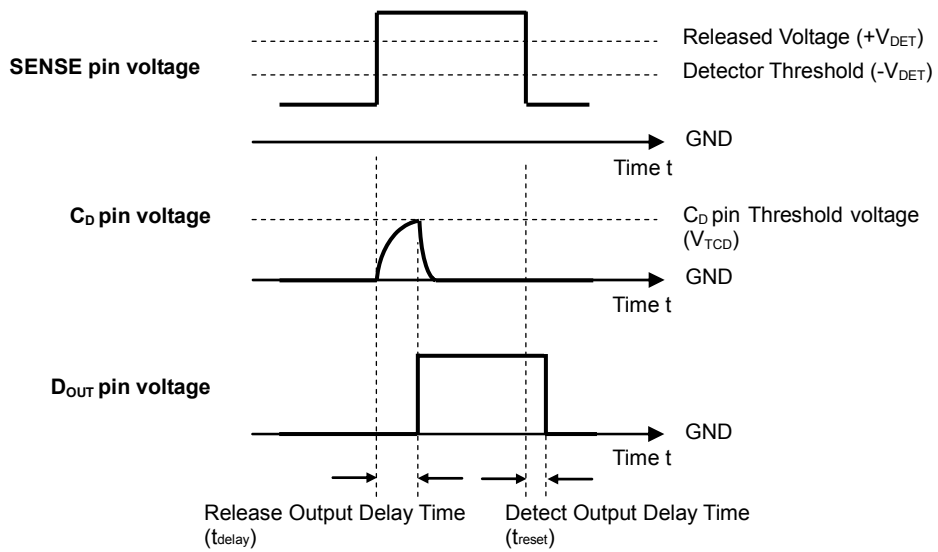
#### RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## TIMING CHART



## DESCRIPTION OF OUTPUT DELAY OPERATION



Output Delay Operation Diagram

## DEFINITION OF OUTPUT DELAY TIME

A higher voltage than the released voltage is forced to the SENSE pin, charge to the capacitor connected to C<sub>D</sub> pin is started, then the C<sub>D</sub> pin voltage increases. Until C<sub>D</sub> pin voltage reaches to C<sub>D</sub> pin threshold voltage, the output of D<sub>OUT</sub> pin voltage keeps "L", then when C<sub>D</sub> pin voltage is higher than C<sub>D</sub> pin threshold voltage, the D<sub>OUT</sub> pin voltage changes from "L" to "H". The released output delay time means the time interval from when the released voltage threshold or more voltage level is forced to SENSE pin to when D<sub>OUT</sub> voltage changes from "L" to "H".

When the voltage of D<sub>OUT</sub> pin reverses from "L" to "H", the discharge of the external capacitor connected to C<sub>D</sub> pin starts. Therefore, the time interval from when the voltage lower than the detector threshold is forced to SENSE pin, to when the output voltage reverses from "H" to "L", or detector output delay time is constant and independent from the external capacitance value.

- \*1. After the D<sub>OUT</sub> pin voltage reverses from "L" to "H", if a voltage lower than the detector threshold is forced to SENSE pin before the capacitor connected to C<sub>D</sub> pin is discharged, delay time will increase. The time interval (t<sub>DIS</sub>) from when the capacitor connected to C<sub>D</sub> pin is discharged completely to when the capacitor is charged to a certain C<sub>D</sub> pin voltage (described as V<sub>CD</sub> herein) can be calculated by power supply voltage (V<sub>DD</sub>), external capacitance (C<sub>D</sub>), on resistance of the C<sub>D</sub> pin discharge transistor (R<sub>DIS</sub>) as in the next formula:

$$t_{DIS} = -R_{DIS} \times C_D \times \ln(V_{CD}/V_{DD} \times 0.45)$$

- \*2. During the released delay operation, only a small current will charge the external capacitor connected to C<sub>D</sub> pin. If the leakage current between C<sub>D</sub> pin and GND is large, the released delay time may increase or the detector may not be released.
- \*3. During the released delay operation, if the V<sub>DD</sub> pin voltage varies, the released output delay time will be also shift.

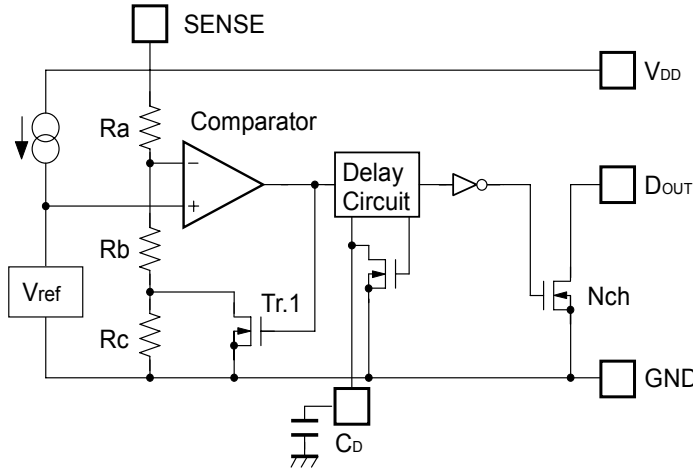
### • How to calculate the released output delay time

The release output delay time (t<sub>delay</sub>) can be calculated as in the next formula with an external capacitance value (C<sub>D</sub>):

$$t_{delay}(s) = 4.545 \times 10^6 \times C_D(F)$$

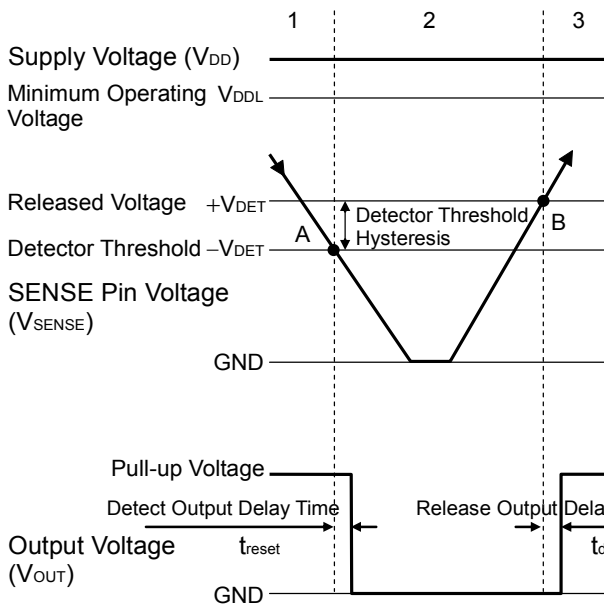
## OPERATION

### • Operation of R3118xxxxA



\*)D<sub>OUT</sub> pin should be pulled-up to V<sub>DD</sub> or an external voltage level.

Block diagram with an external capacitor (R3118xxxxA)



Step	1	2	3
Comparator (-) Pin Input Voltage	I	II	I
Comparator Output	L	H	L
Tr.1	OFF	ON	OFF
Output Tr. Nch	OFF	ON	OFF

$$I \quad \frac{R_b+R_c}{R_a+R_b+R_c} \times V_{SENSE}$$

$$II \quad \frac{R_b}{R_a+R_b} \times V_{SENSE}$$

Operation Diagram

### • Explanation of operation

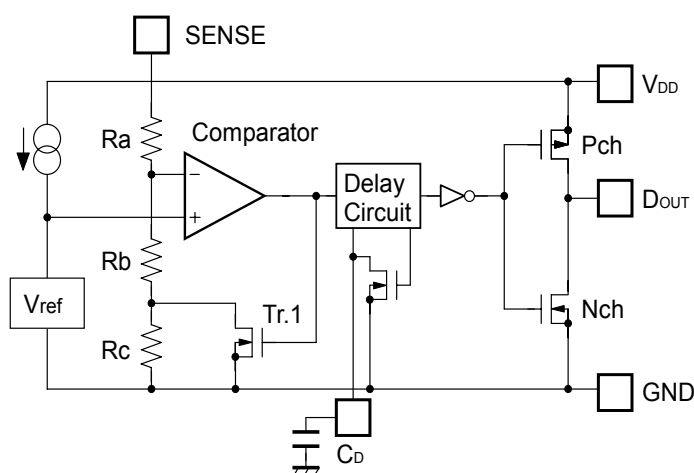
Step 1. The output voltage is equal to the pull-up voltage.

Step 2. At Point "A",  $V_{ref} \leq V_{SENSE} \times (R_b+R_c) / (R_a+R_b+R_c)$  is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage (-V<sub>DET</sub>). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

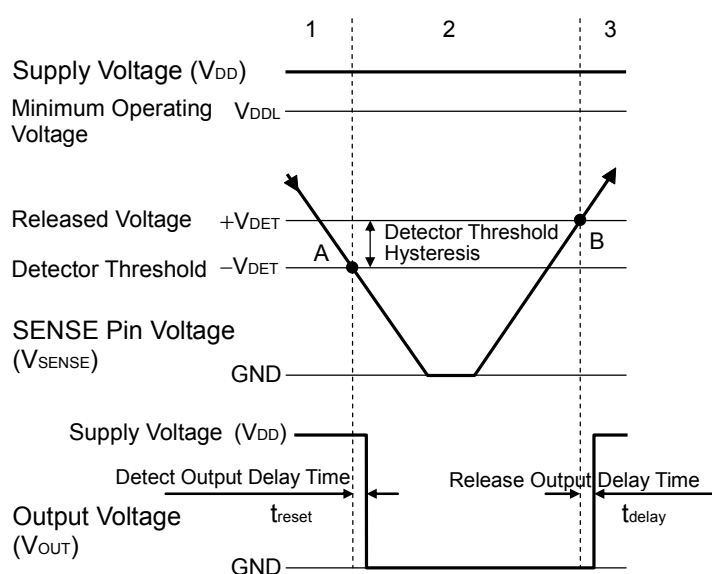
Step 3. At Point "B",  $V_{ref} \leq V_{SENSE} \times R_b / (R_a+R_b)$  is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the pull-up voltage. The voltage level of Point B means a released voltage (+V<sub>DET</sub>).

\*) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

## • Operation of R3118xxxxC



Block diagram with an external capacitor (R3118xxxxC)



Step	1	2	3	
Comparator (-) Pin Input Voltage	I	II	I	
Comparator Output	L	H	L	
Tr.1	OFF	ON	OFF	
Output Tr.	Pch	ON	OFF	ON
	Nch	OFF	ON	OFF

$$I \quad \frac{R_b + R_c}{R_a + R_b + R_c} \times V_{SENSE}$$

$$II \quad \frac{R_b}{R_a + R_b} \times V_{SENSE}$$

Operation Diagram

## • Explanation of operation

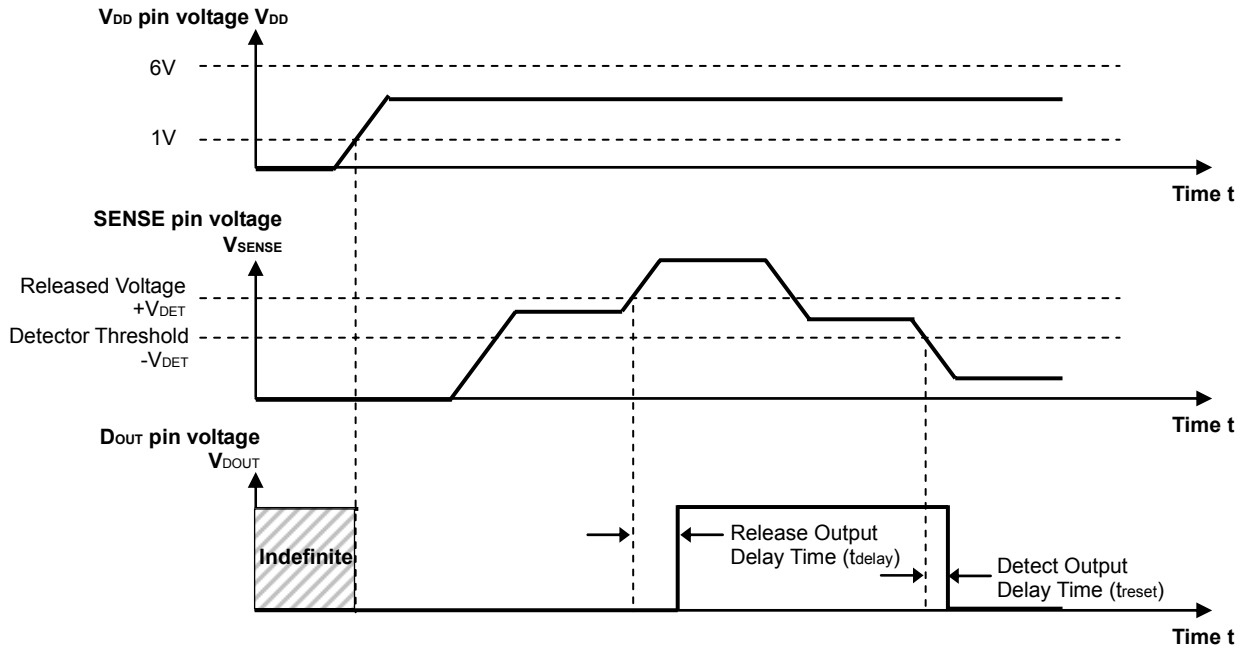
Step 1. The output voltage is equal to the supply voltage ( $V_{DD}$ ).

Step 2. At Point "A",  $V_{ref} \geq V_{SENSE} \times (R_b + R_c) / (R_a + R_b + R_c)$  is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ( $-V_{DET}$ ). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

Step 3. At Point "B",  $V_{ref} \leq V_{SENSE} \times R_b / (R_a + R_b)$  is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the supply voltage ( $V_{DD}$ ). The voltage level of Point B means a released voltage ( $+V_{DET}$ ).

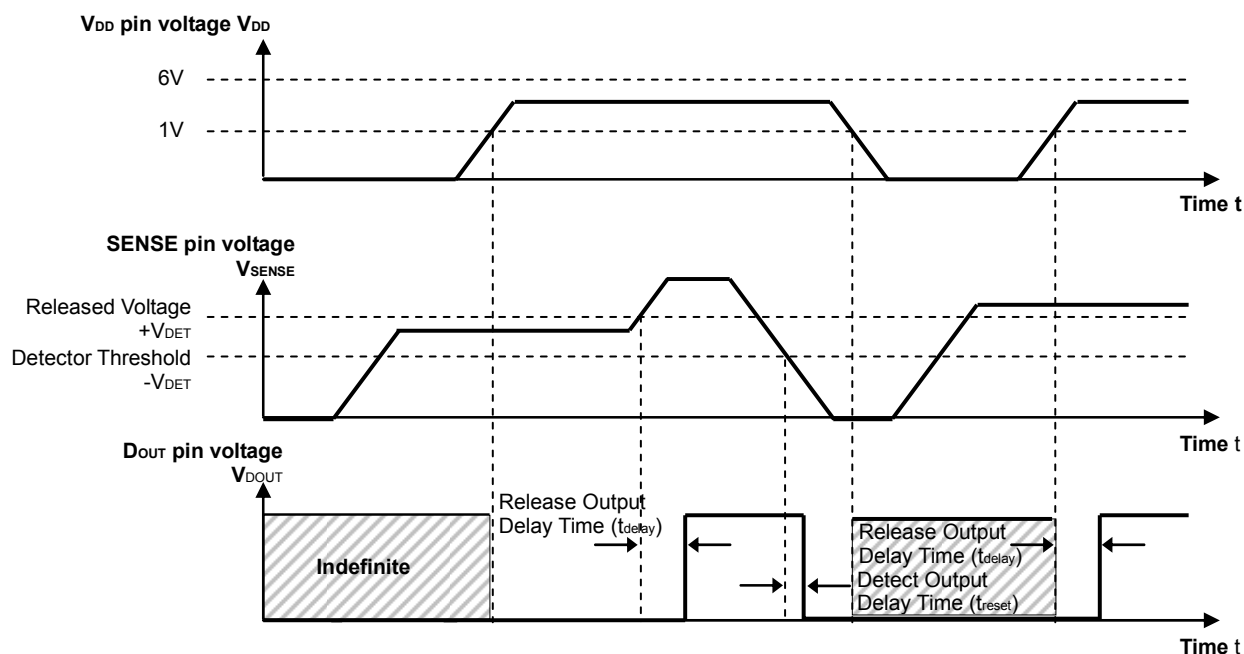
\*) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

- In case of the SENSE pin voltage is forced after the V<sub>DD</sub> pin voltage is forced.



If a power supply (in the range from 1V to 6V) is forced to V<sub>DD</sub> pin and a voltage is forced to SENSE pin, when the SENSE pin voltage is less than released voltage +V<sub>DET</sub>, D<sub>OUT</sub> pin becomes "L". When the SENSE pin voltage is equal or more than the released voltage +V<sub>DET</sub>, D<sub>OUT</sub> pin becomes "H".

- In case of the  $V_{DD}$  pin voltage is forced after the SENSE pin voltage is forced.



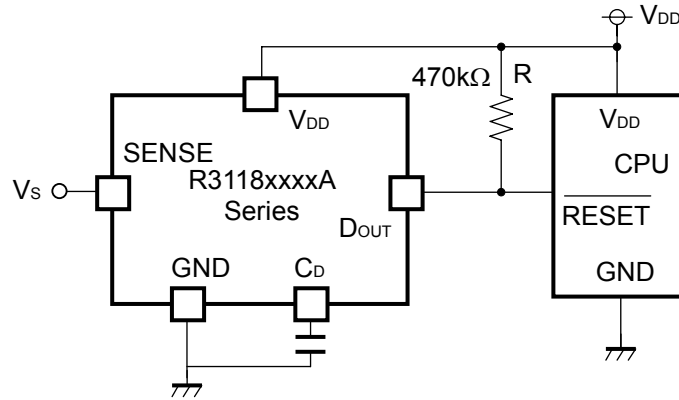
In the case of the SENSE pin voltage is less than released voltage  $+V_{DET}$ , when the  $V_{DD}$  pin voltage becomes to 1V or more, "L" output of  $D_{OUT}$  is determined. In case of the SENSE pin voltage is equal or more than the released voltage  $+V_{DET}$ , when the  $V_{DD}$  pin voltage becomes to 1V or more, "H" output of  $D_{OUT}$  is determined.

\*) If the turn on speed of the supply voltage of the  $V_{DD}$  pin up to 1V is slower than the 1V/s, connect 0.001 $\mu$ F or more capacitor to  $C_D$  pin, otherwise, the output of  $D_{OUT}$  pin may indefinite.

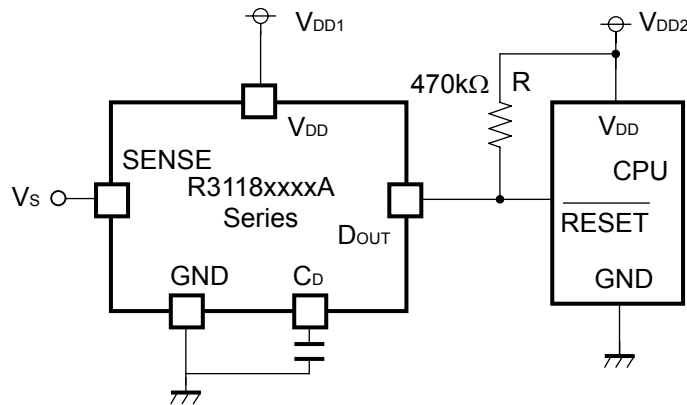
## TYPICAL APPLICATION

- R3118xxxxA CPU Reset Circuit (Nch Open Drain Output)

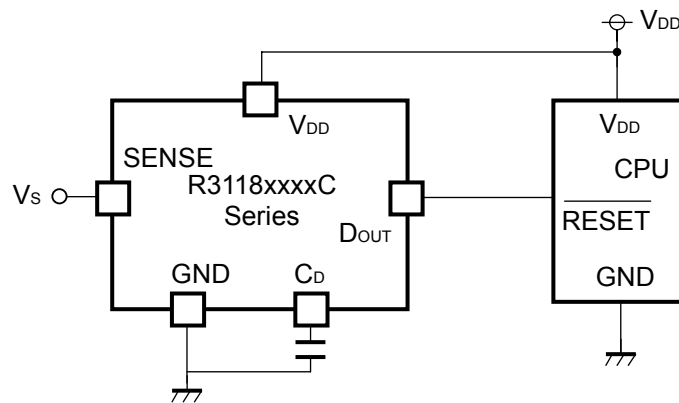
(1)  $V_{DD}$  pin Voltage to R3118xxxxA is equal to  $V_{DD}$  pin Voltage to CPU



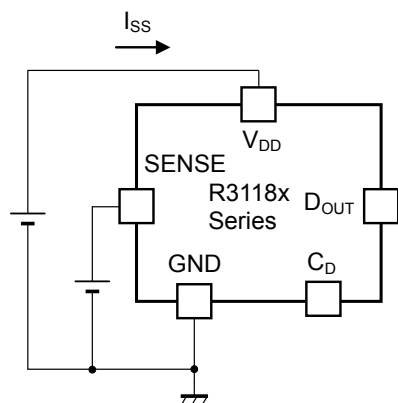
(2)  $V_{DD}$  pin Voltage to R3118xxxxA is unequal to  $V_{DD}$  pin Voltage to CPU



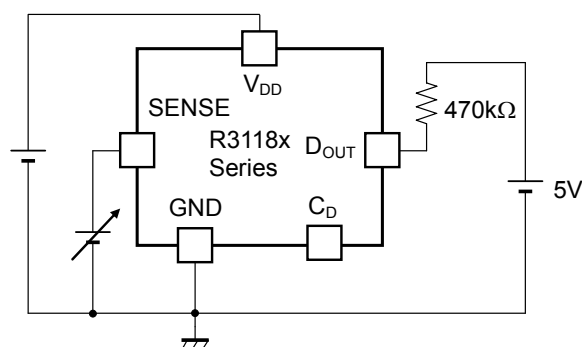
- R3118xxxxC CPU Reset Circuit (CMOS Output)



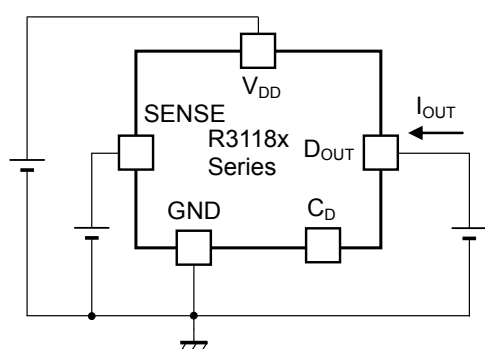
## TEST CIRCUITS



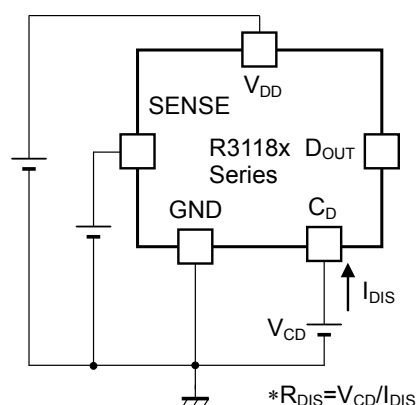
**Supply Current Test Circuit**



**Detector Threshold Test Circuit**  
(Pull-up circuit is not necessary for CMOS Output type.)

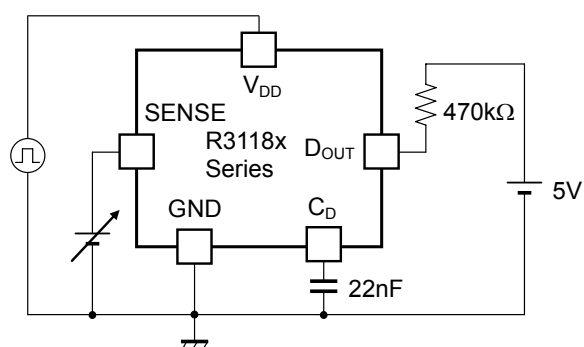


**Nch/Pch Driver Output Current Test Circuit**



$$*R_{DIS} = V_{CD} / I_{DIS}$$

**C<sub>D</sub> pin Discharge Transistor On resistance Test Circuit**

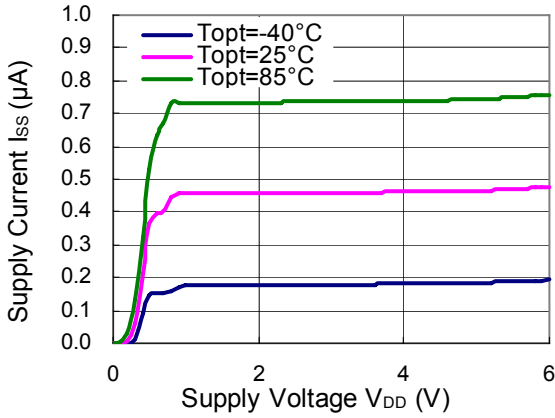


**Detect output delay time/Release output delay time Test Circuit**  
(Pull-up circuit is not necessary for CMOS Output type.)

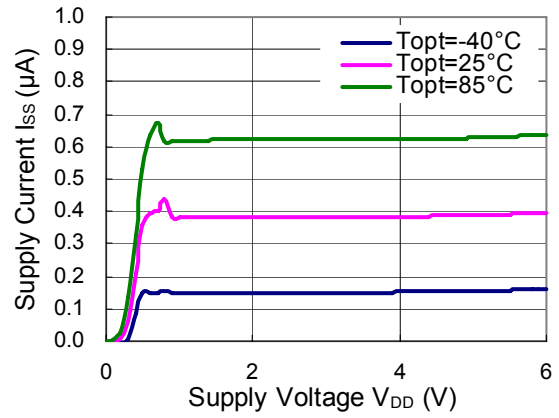
## TYPICAL CHARACTERISTICS

### 1) Supply Current vs. Supply Voltage

R3118xxxxA/C ( $V_{SENSE}=0V$ )

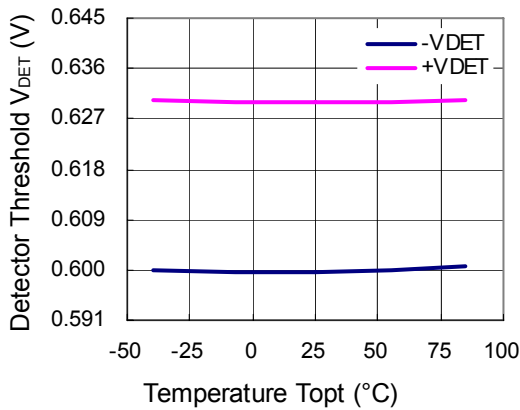


R3118xxxxA/C ( $V_{SENSE}=6V$ )

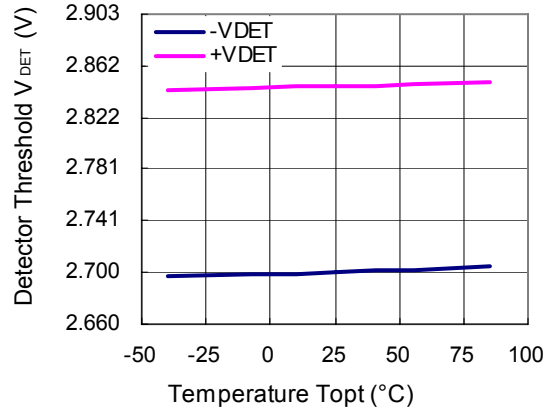


### 2) Detector Threshold vs. Temperature

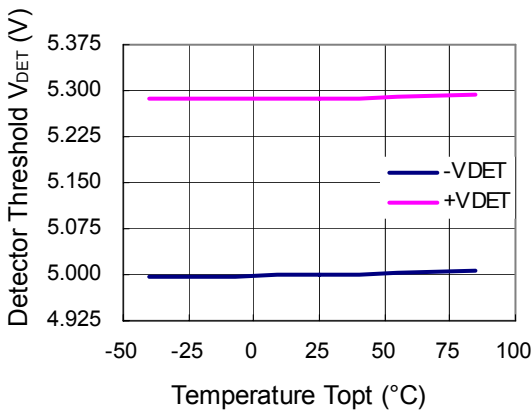
R3118x06xA/C ( $V_{DD}=5.3V$ )



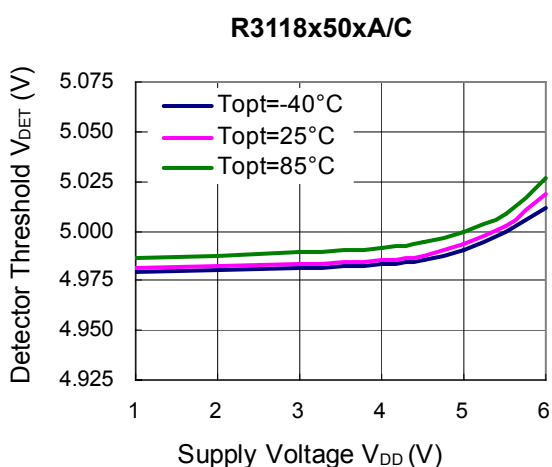
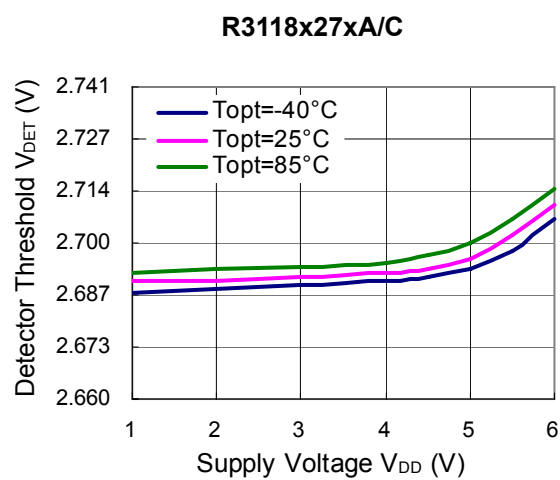
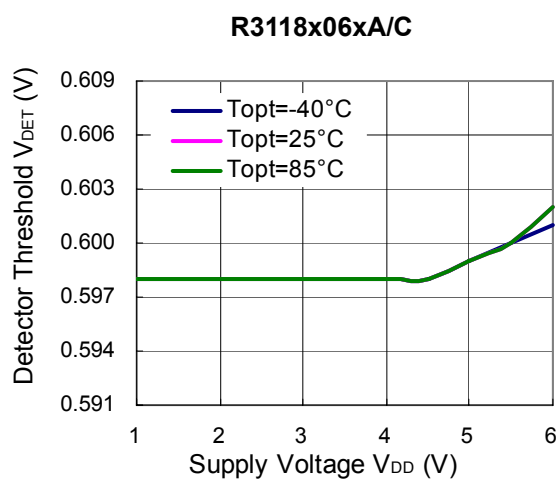
R3118x27xA/C ( $V_{DD}=5.3V$ )



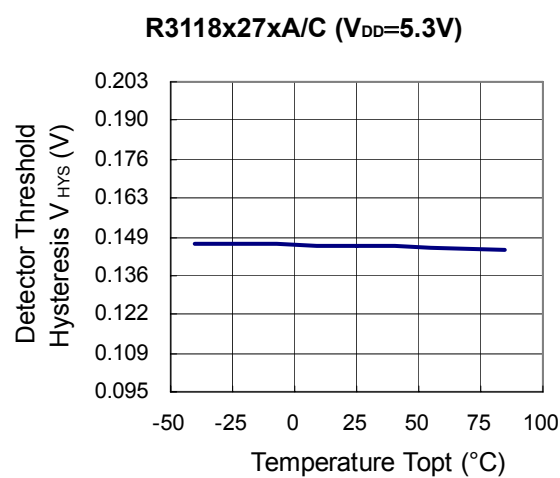
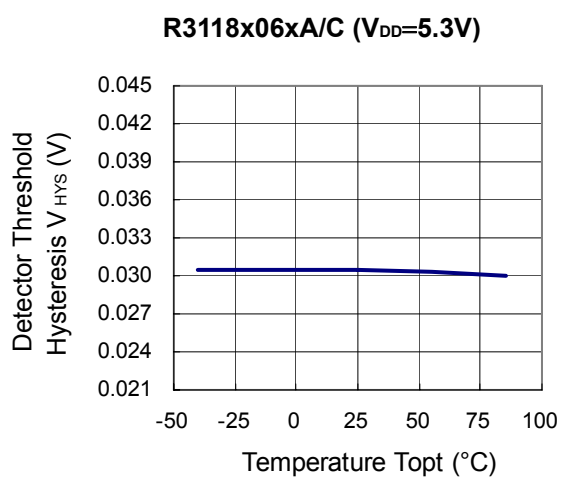
R3118x50xA/C ( $V_{DD}=5.3V$ )



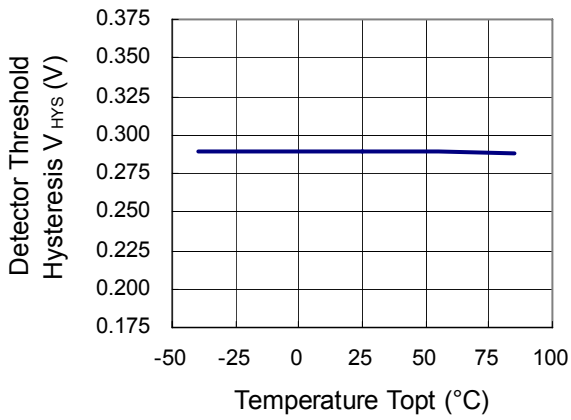
### 3) Detector Threshold vs. Supply Voltage



### 4) Hysteresis vs. Temperature

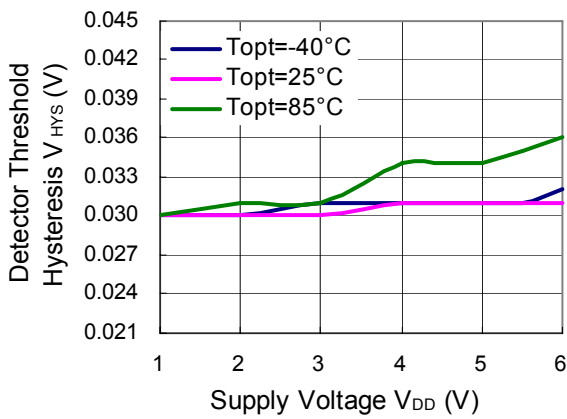


R3118x50xA/C ( $V_{DD}=5.3V$ )

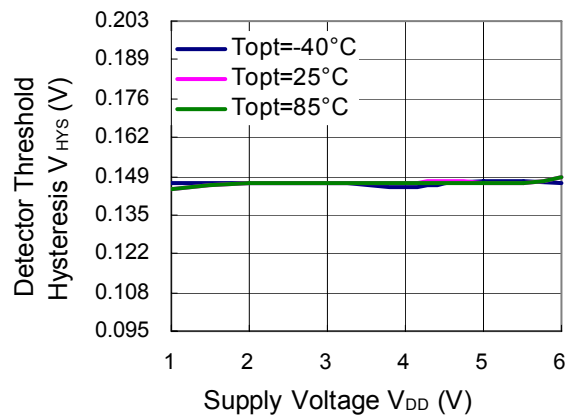


5) Hysteresis vs. Supply Voltage

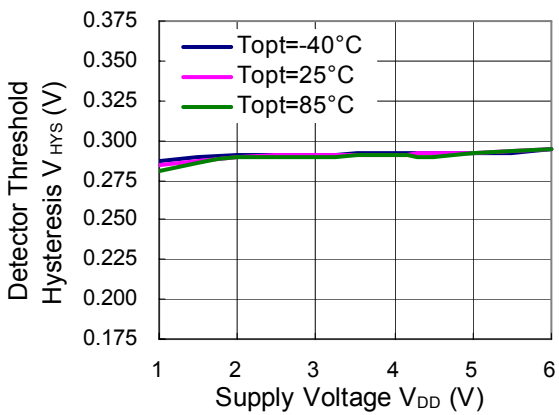
R3118x06xA/C



R3118x27xA/C

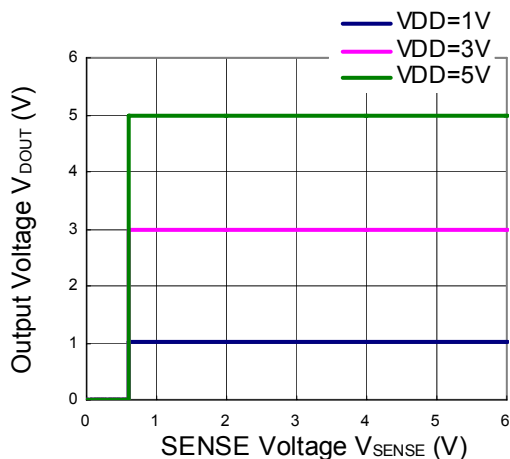


R3118x50xA/C

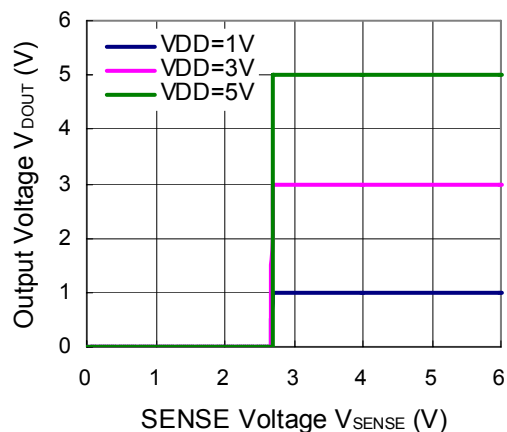


6) Output Voltage vs. SENSE Voltage (Dout pin is pulled up to V<sub>DD</sub> pin via 470kΩ.)

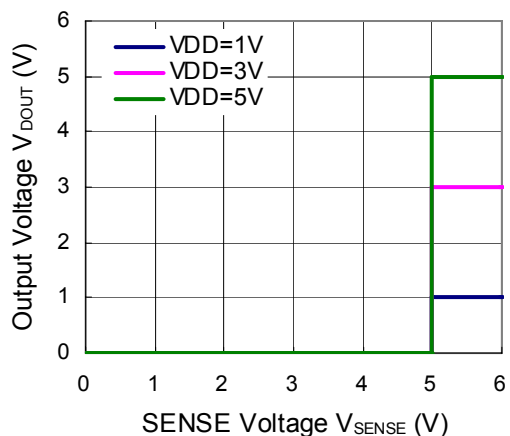
R3118x06xA/C



R3118x27xA/C

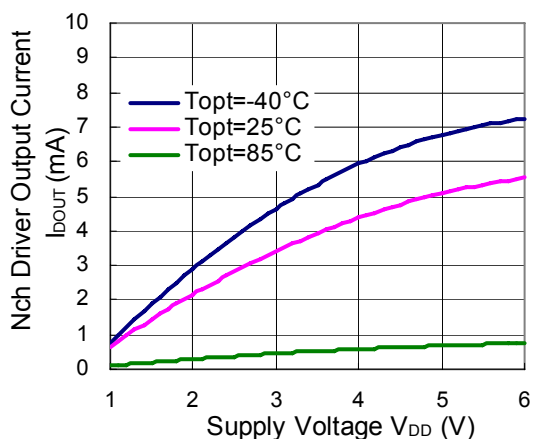


R3118x50xA/C



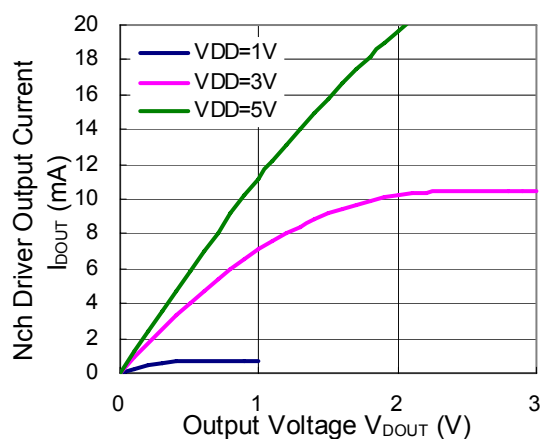
7) Nch Driver Output Current vs. Supply Voltage

R3118xxxxA/C (V<sub>DOUT</sub>=0.4V)



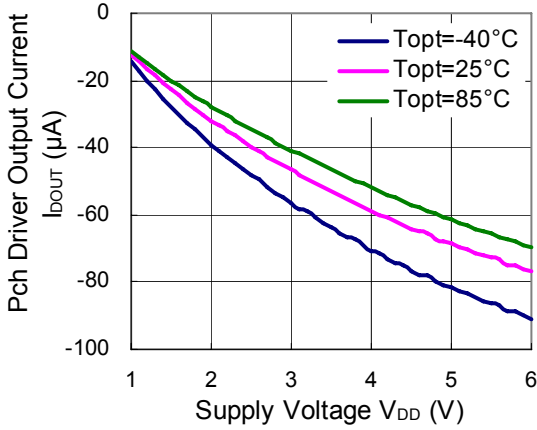
8) Nch Driver Output Current vs. Output Voltage

R3118xxxxA/C



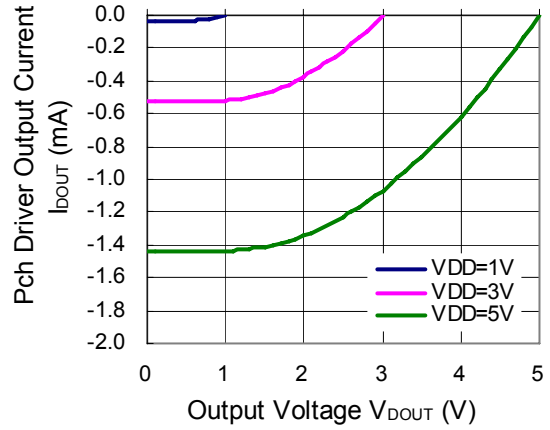
9) Pch Driver Output Current vs. Supply Voltage

R3118xxxxA/C ( $V_{DOUT}=V_{DD}-0.1V$ )



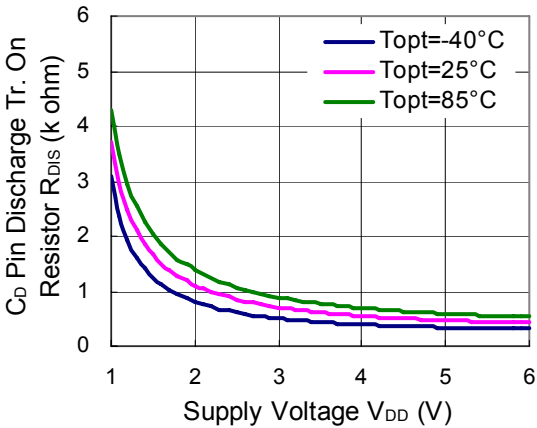
10) Pch Driver Output current vs. Output voltage

R3118xxxxA/C



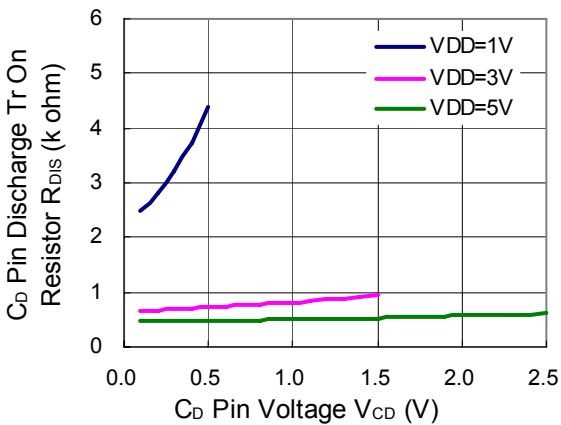
11) C<sub>D</sub> pin Discharge Tr. On Resistance vs. Supply Voltage

R3118xxxxA/C ( $V_{CD}=0.4V$ )



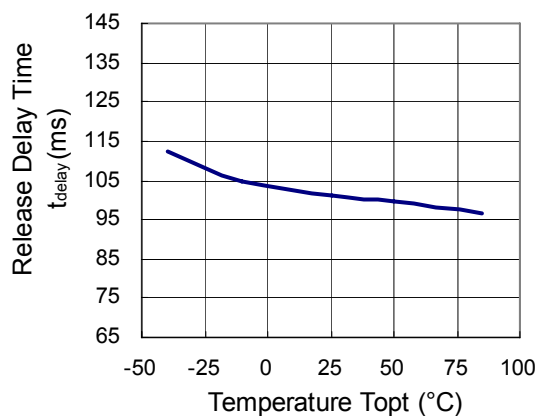
12) C<sub>D</sub> pin Discharge Transistor On Resistance vs. C<sub>D</sub> pin voltage

R3118xxxxA/C



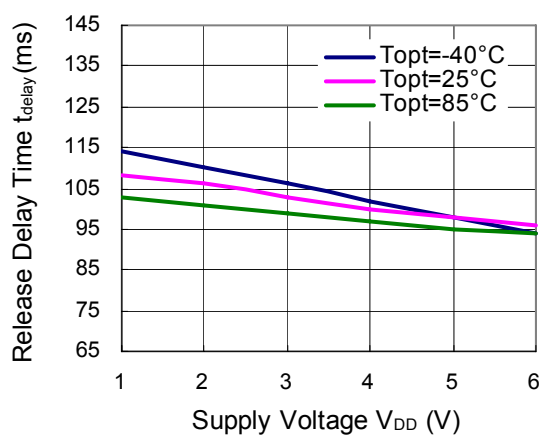
### 13) Release Output Delay Time vs. Temperature

R3118xxxxA/C ( $V_{DD}=4V$ ,  $C_D=0.022\mu F$ )



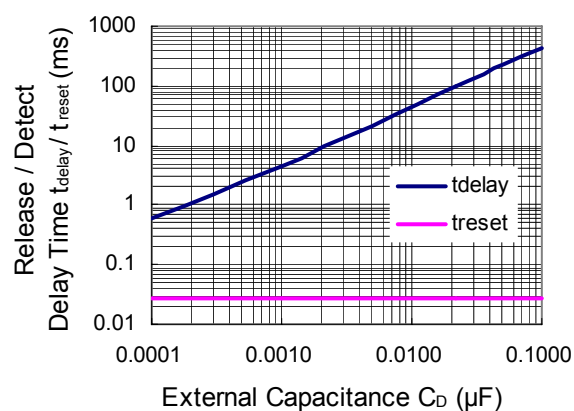
### 14) Release Output Delay Time vs. Supply Voltage

R3118xxxxA/C ( $C_D=0.022\mu F$ )

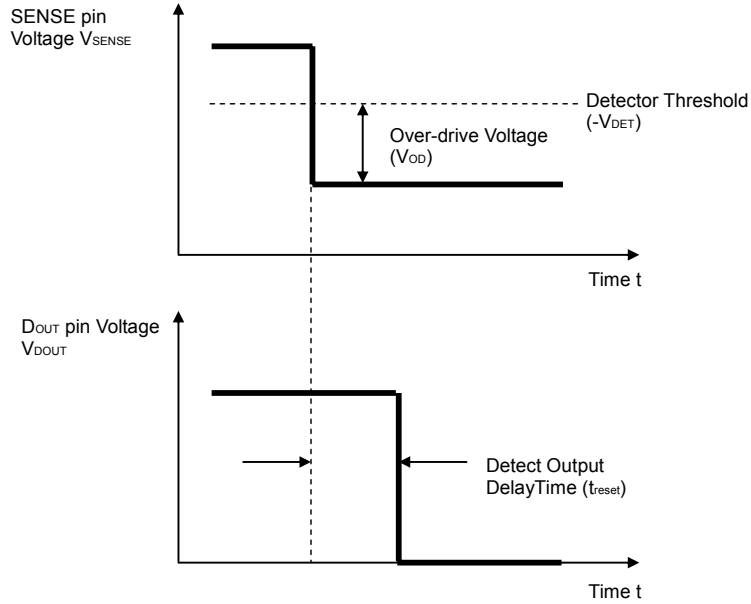


### 15) Detect Output Delay Time/Release Output Delay Time vs. $C_D$ pin External Capacitance

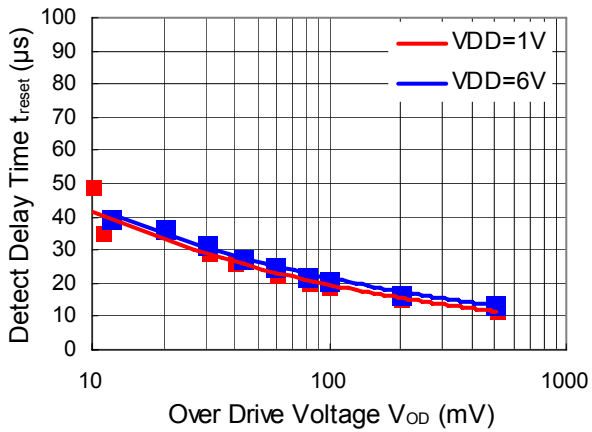
R3118xxxxA/C ( $V_{DD}=4V$ )



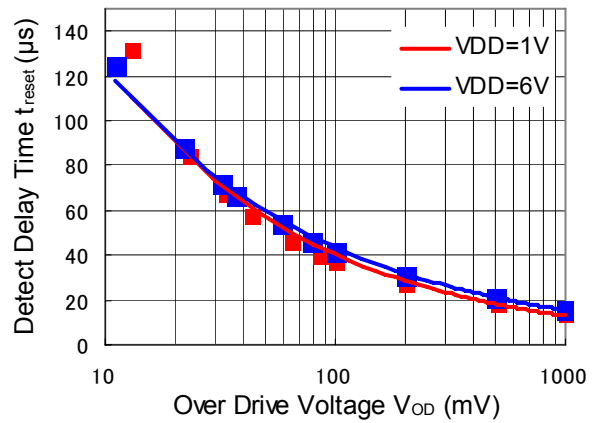
16) Detect Output Delay time vs. Over-drive Voltage



R3118x06xA/C ( $C_D=none$ )

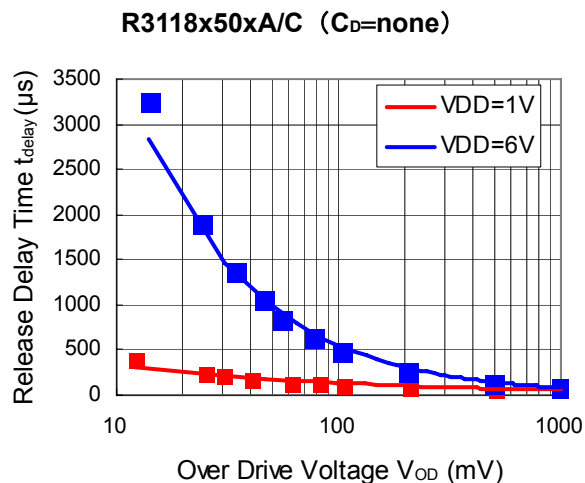
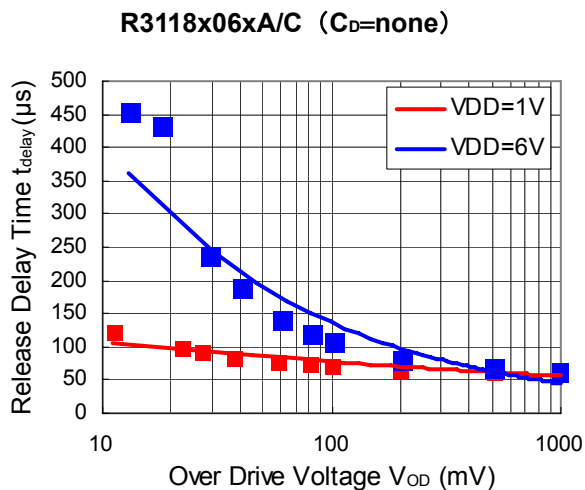
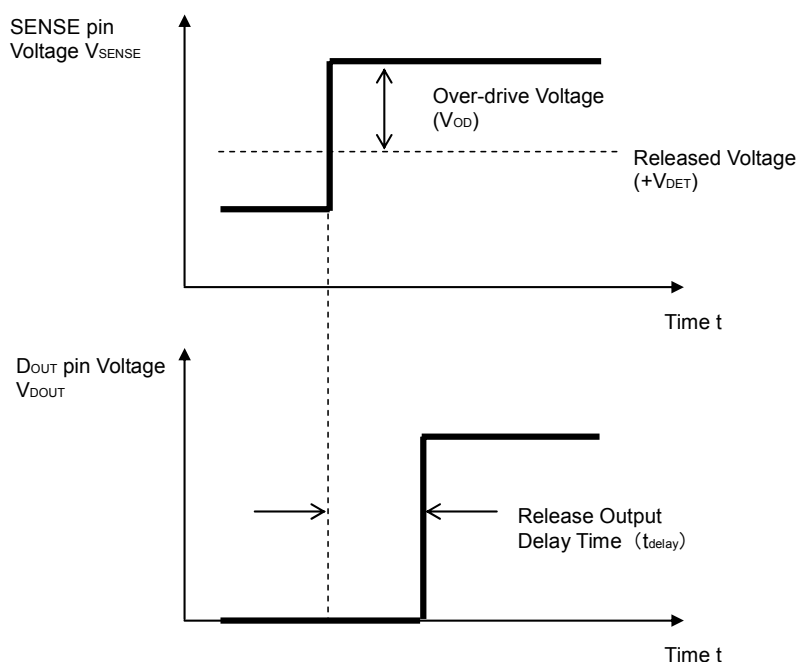


R3118x50xA/C ( $C_D=none$ )



The pulse shorter than the detect output delay time cannot be detected, and "L" does not output from D\_OUT pin.

## 17) Release Output Delay time vs. Over-drive Voltage



- If the pulse is shorter than the output release delay time, the R3118 cannot be released and "H" does not output from  $D_{OUT}$  pin.
- If the attachment capacitor for  $C_D$  pin for setting a delay time is too small and the difference between the released voltage threshold and the actual released voltage is too small or the slope for rising voltage of the SENSE pin is too slow, the output delay time tolerance will be worse.

Ex. Attachment capacitor=0.0001 $\mu$ F, Released voltage threshold=4.725V, Actual released voltage=4.75V In this case, the calculated delay time=0.4545ms, however, over-drive voltage is only 25mV. Therefore, the actual delay time will be approximately 2.4545ms. If the attachment capacitor=0.001 $\mu$ F and other conditions are same as above, the calculated delay time=4.545ms, and the actual delay time will be approximately 6.545ms. If the attachment capacitor=0.01 $\mu$ F and other conditions are same as above, the calculated delay time=45.45ms, and the actual delay time will be approximately 47.45ms.

## TECHNICAL NOTES

When R3118xxxxA/C is used in the circuit as SENSE pin and  $V_{DD}$  pin are connected each other such as in Fig. A, if the value of R1 is set excessively large, the dropdown voltage caused by the consumption current of IC itself, may vary the detector threshold and the released voltage. Also, if the value of R1 is set excessively large, there may cause oscillation generated by cross conduction current with released operation. If the R1 value is more than  $V_{HYS}/0.25(k\Omega)$ , the detector may not released.

In the case that the R3118xxxxA/C is used in the circuit as SENSE pin and  $V_{DD}$  pin are connected each other such as in Fig.B, if the value of R1 is set excessively large, there may cause the shift of released output delay time or oscillation generated by the cross conduction current with released operation.

In the case that the R3118xxxxA is used in the circuit such as in Fig.C, if R1 value is small,  $D_{OUT}$  pin voltage at detector may rise. In the case that the R3118xxxxC is used in the circuit such as in Fig.C, current may flow from  $V_{DD}$  pin to  $D_{OUT}$  pin, or from  $D_{OUT}$  pin to  $V_{DD}$  pin.

In the case that the R3118xxxxC is used in the circuit such as in Fig.D, if R1 value is small,  $D_{OUT}$  pin voltage at release may drop.

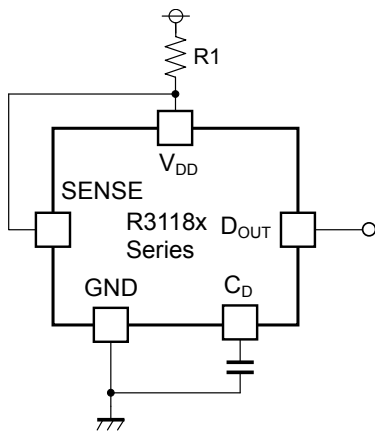


Fig. A

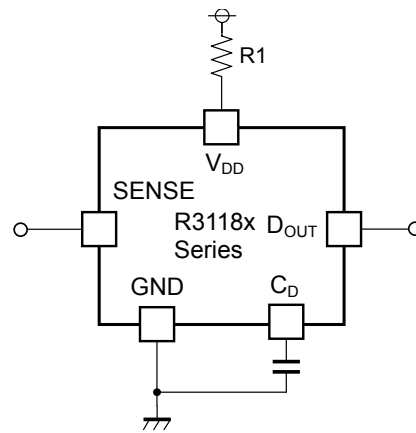


Fig. B

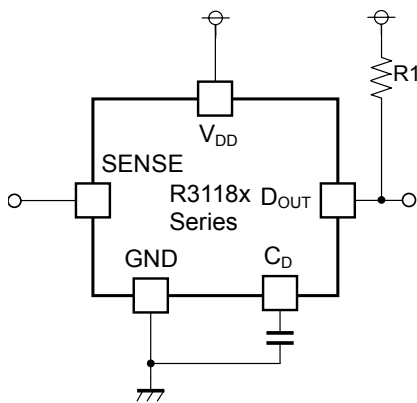


Fig. C

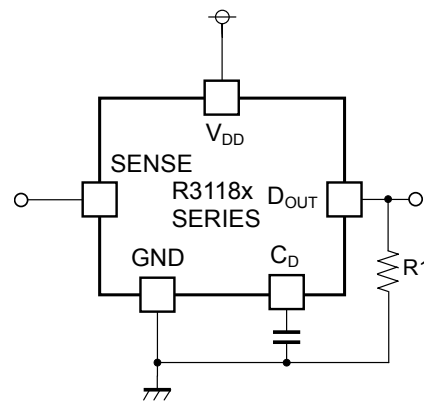


Fig. D



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