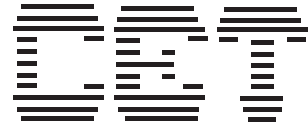


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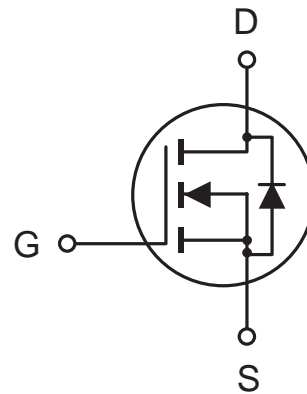
PRELIMINARY

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## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 20V , 25A ,  $R_{DS(ON)}=40m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=70m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous -Pulsed	I <sub>D</sub>	25	A
	I <sub>DM</sub>	75	A
Drain-Source Diode Forward Current	I <sub>S</sub>	25	A
Maximum Power Dissipation @T <sub>c</sub> =25°C Derate above 25°C	P <sub>D</sub>	43	W
		0.29	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	3.5	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

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## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.5		1.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 8A		30	40	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 6.6A		55	70	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 4.5V	25			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 8A		15		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V f = 1.0MHz		511		pF
Output Capacitance	C <sub>OSS</sub>			216		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			73		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 10V, I <sub>D</sub> = 1A V <sub>GS</sub> = 4.5V, R <sub>GEN</sub> = 6Ω		20	50	ns
Rise Time	t <sub>r</sub>			12	30	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			50	100	ns
Fall Time	t <sub>f</sub>			10	25	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 8A V <sub>GS</sub> = 4.5V		11	15	nC
Gate-Source Charge	Q <sub>gs</sub>			3.6		nC
Gate-Drain Charge	Q <sub>gd</sub>			2.8		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_s = 4\text{A}$			1.3	V

Notes

a. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

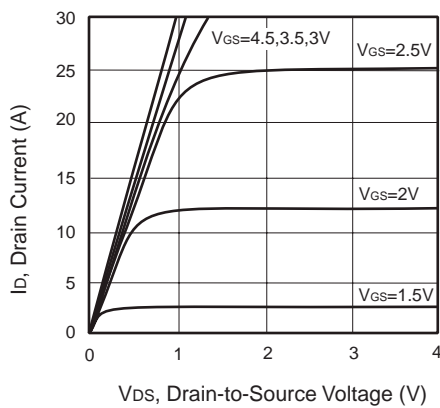


Figure 1. Output Characteristics

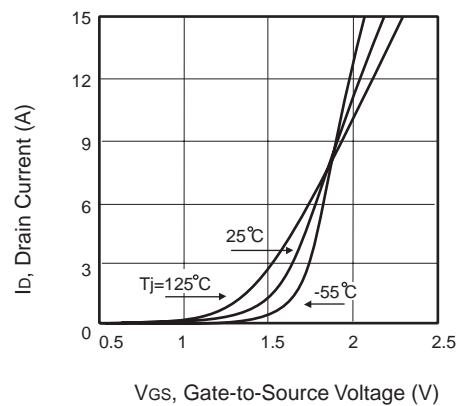


Figure 2. Transfer Characteristics

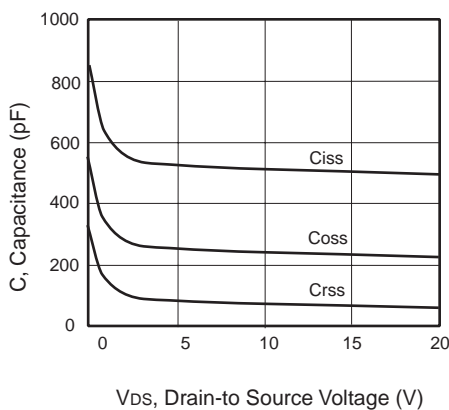


Figure 3. Capacitance

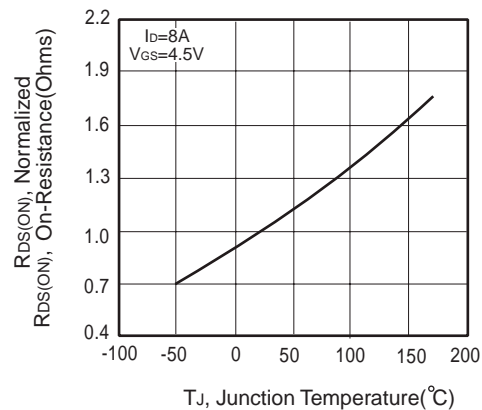
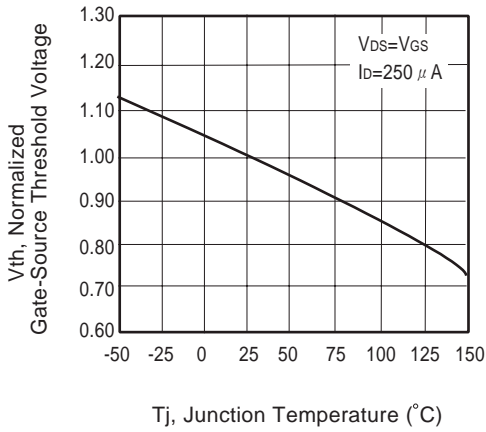


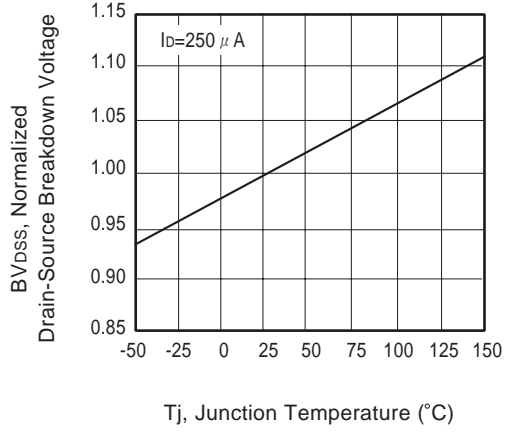
Figure 4. On-Resistance Variation with Temperature

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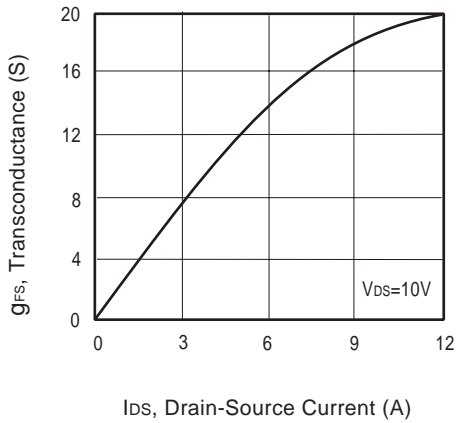
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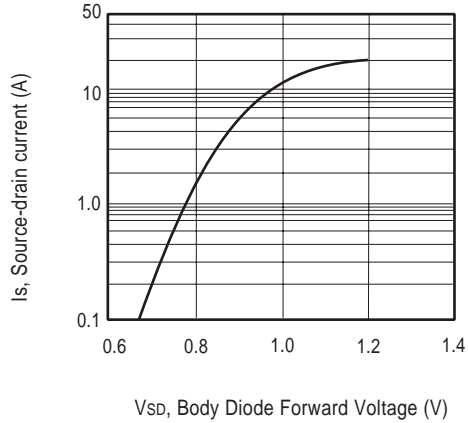
**Figure 5. Gate Threshold Variation with Temperature**



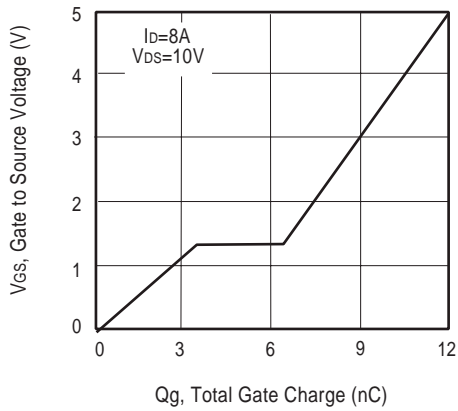
**Figure 6. Breakdown Voltage Variation with Temperature**



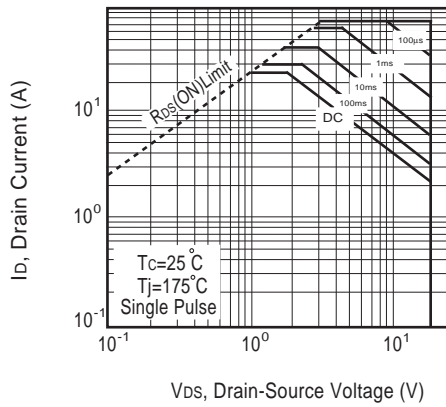
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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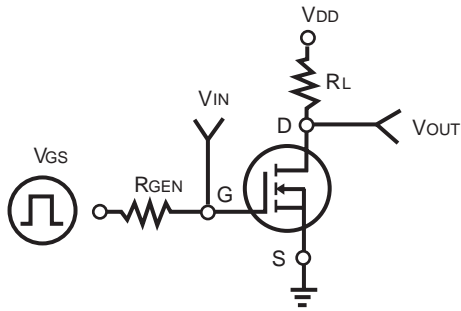


Figure 11. Switching Test Circuit

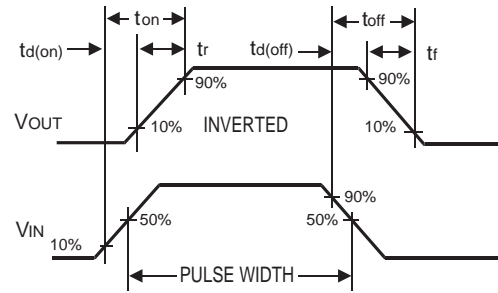


Figure 12. Switching Waveforms

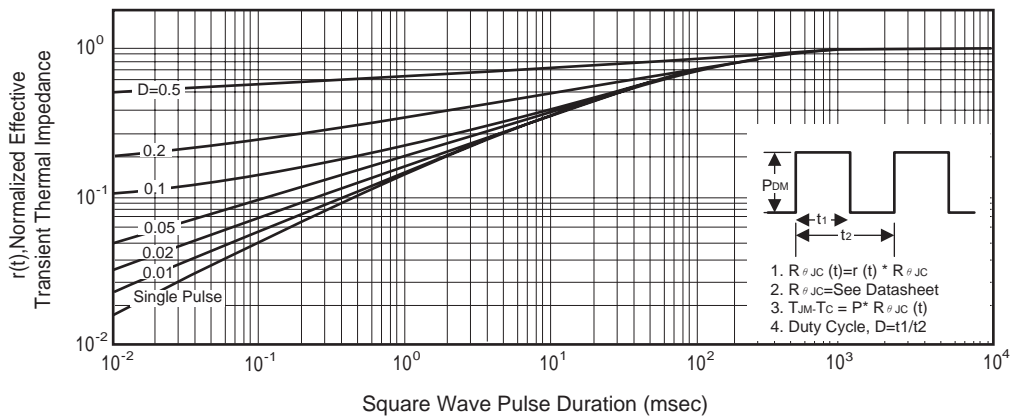


Figure 13. Normalized Thermal Transient Impedance Curve