



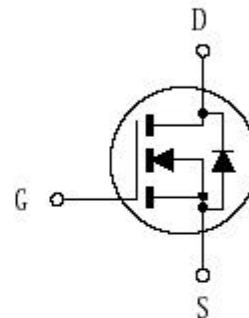
CED703AL/CEU703AL

PRELIMINARY

N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- ◆ 30V , 40A , $R_{DS(ON)}=19m\Omega$ @ $V_{GS}=10V$,
 $R_{DS(ON)}=30m\Omega$ @ $V_{GS}=4.5V$.
- ◆ Super high dense cell design for extremely low $R_{DS(ON)}$.
- ◆ High power and current handling capability.
- ◆ TO-220 & TO-263 package.



6

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous ^a @ $T_J=125^\circ\text{C}$ -Pulsed	I_D	40	A
	I_{DM}	120	A
Drain-Source Diode Forward Current ^a	I_S	40	A
Maximum Power Dissipation ^a @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	50	W
		0.3	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

6

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			10	μA
Gate-Body Leakage	I_{SS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1		3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 25A$		15	19	n Ω
		$V_{GS} = 4.5V, I_D = 10A$		23	32	n Ω
On-State Drain Current	$I_{D(on)}$	$V_{GS} = 10V, V_{DS} = 10V$	60			A
Forward Transconductance	g_{FS}	$V_{DS} = 10V, I_D = 25A$		30		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V$ $f = 1.0MHz$		1000		pF
Output Capacitance	C_{oss}			420		pF
Reverse Transfer Capacitance	C_{rss}			100		pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	$t_{D(on)}$	$V_{DD} = 15V,$ $I_D = 25A,$ $V_{GS} = 10V,$ $R_{\theta J-C} = 24 \Omega$		18	23	ns
Rise Time	t_r			120	180	ns
Turn-Off Delay Time	$t_{D(off)}$			80	120	ns
Fall Time	t_f			60	165	ns
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 25A,$ $V_{GS} = 5V$		15	20	nC
Gate-Source Charge	Q_{gs}			4		nC
Gate-Drain Charge	Q_{gd}			6		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_S = 25\text{A}$		0.93	1.3	V

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Notes

- a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

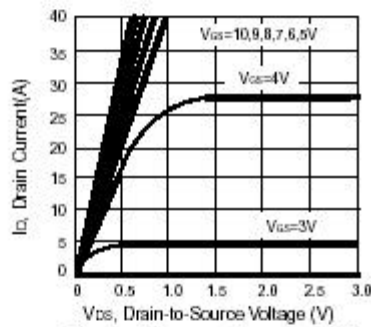


Figure 1. Output Characteristics

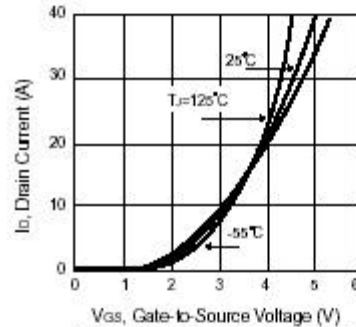


Figure 2. Transfer Characteristics

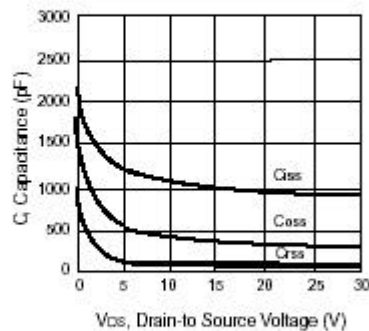


Figure 3. Capacitance

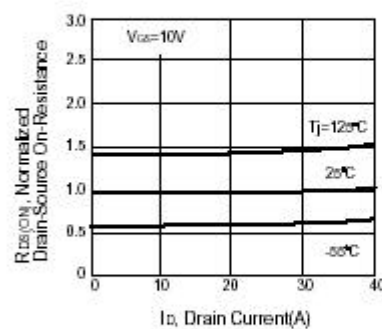


Figure 4. On-Resistance Variation with Drain Current and Temperature

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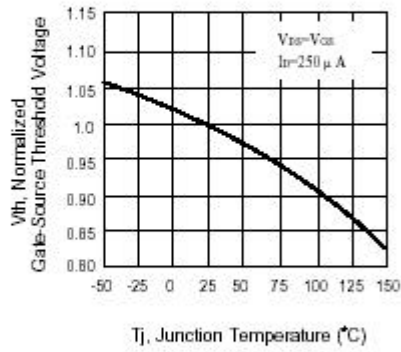


Figure 5. Gate Threshold Variation with Temperature

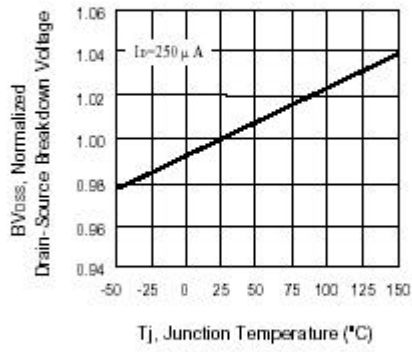


Figure 6. Breakdown Voltage Variation with Temperature

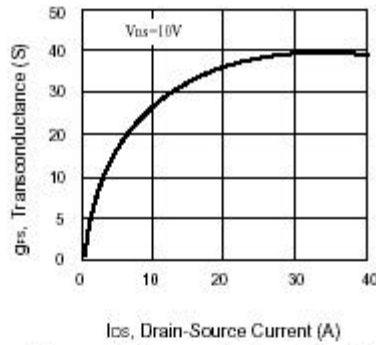


Figure 7. Transconductance Variation with Drain Current

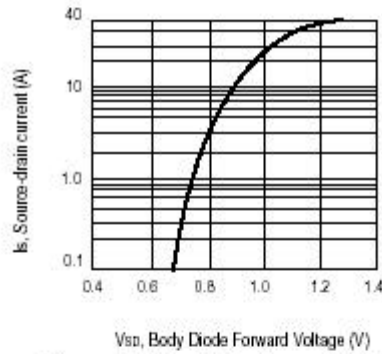


Figure 8. Body Diode Forward Voltage Variation with Source Current

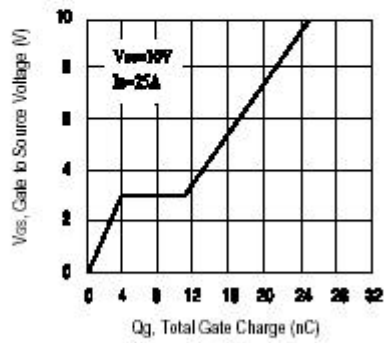


Figure 9. Gate Charge

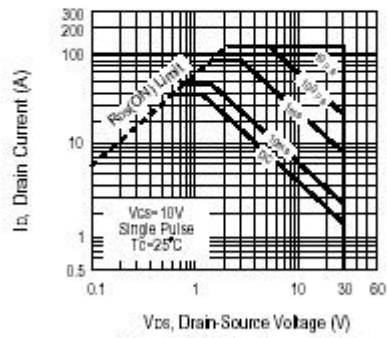


Figure 10. Maximum Safe Operating Area

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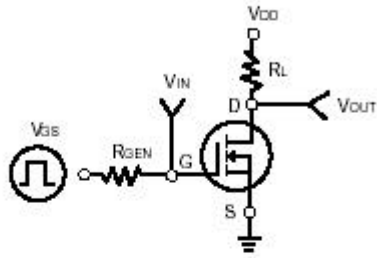


Figure 11. Switching Test Circuit

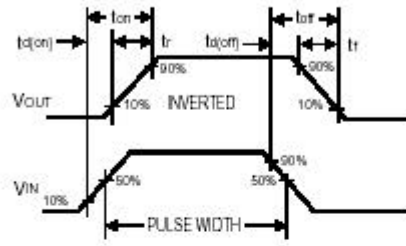


Figure 12. Switching Waveforms

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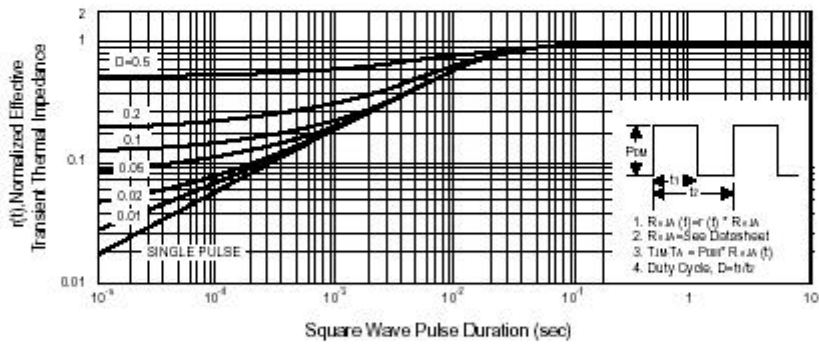


Figure 13. Normalized Thermal Transient Impedance Curve