

# CED4060AL/CEU4060AL



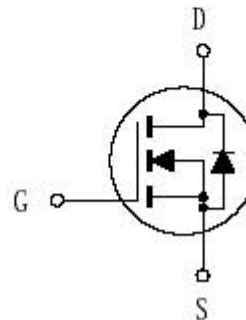
March 1998

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

6

- ◆ 60V , 15A ,  $R_{DS(ON)}=80m\Omega$  @ $V_{GS}=10V$ ,  
 $R_{DS(ON)}=85m\Omega$  @ $V_{GS}=5V$ .
- ◆ Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- ◆ High power and current handling capability.
- ◆ TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Drain Current-Continuous -Pulsed	$I_D$	15	A
	$I_{DM}$	45	A
Drain-Source Diode Forward Current	$I_S$	15	A
Maximum Power Dissipation @Tc=25°C Derate above 25°C	$P_D$	50	W
		0.3	W/°C
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

# CED4060AL/CEU4060AL

## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25<sup>o</sup>C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V			25	μA
Gate-Body Leakage	I <sub>GBS</sub>	V <sub>GS</sub> = ±16V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.5	2	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A		65	80	mΩ
		V <sub>GS</sub> = 5V, I <sub>D</sub> = 6A		79	85	mΩ
On-State Drain Current	I <sub>D(on)</sub>	V <sub>GS</sub> = 5V, V <sub>DS</sub> = 10V	15			A
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		10		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1.0MHz		480		pF
Output Capacitance	C <sub>OSS</sub>			130		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			30		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(on)</sub>	V <sub>DD</sub> = 30V, I <sub>L</sub> = 15A, V <sub>GS</sub> = 5V, R <sub>GS</sub> = 51 Ω,		15	20	ns
Rise Time	t <sub>r</sub>			210	250	ns
Turn-Off Delay Time	t <sub>D(off)</sub>			55	100	ns
Fall time	t <sub>f</sub>			80	150	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 48V, I <sub>D</sub> = 15A, V <sub>DS</sub> = 10V		13	17	nC
Gate-Source Charge	Q <sub>gs</sub>			2.6		nC
Gate-Drain Charge	Q <sub>gd</sub>			3.2		nC

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 6A$		0.83	1.3	V

6

### Notes

a. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

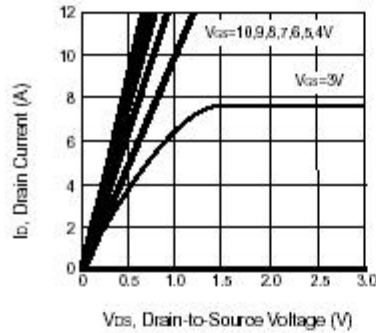


Figure 1. Output Characteristics

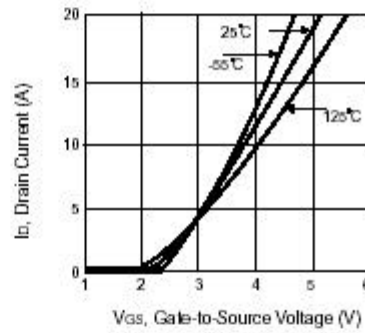


Figure 2. Transfer Characteristics

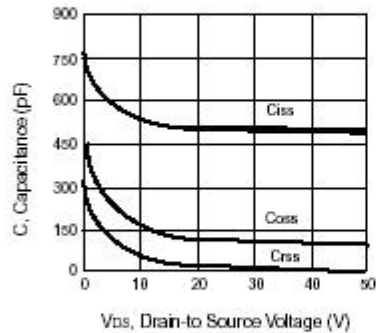


Figure 3. Capacitance

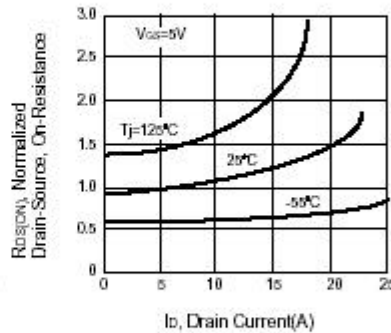
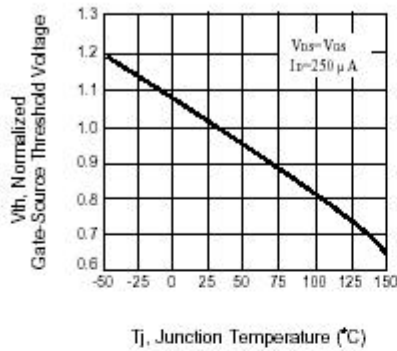


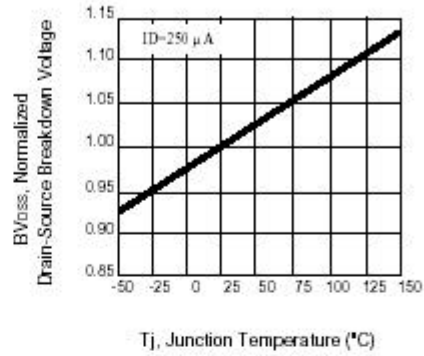
Figure 4. On-Resistance Variation with Drain Current and Temperature

# CED4060AL/CEU4060AL

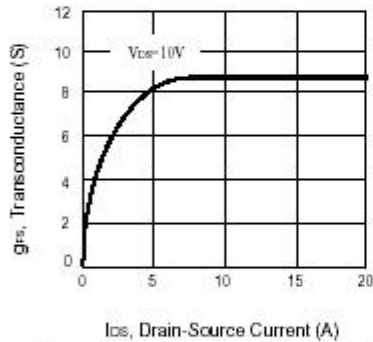
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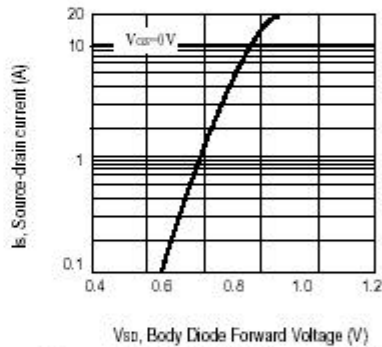
**Figure 5. Gate Threshold Variation with Temperature**



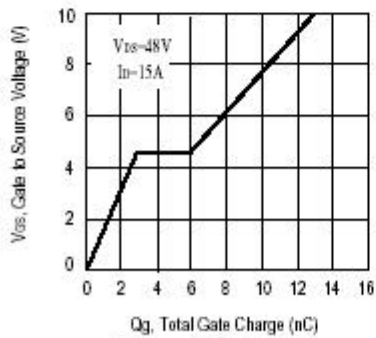
**Figure 6. Breakdown Voltage Variation with Temperature**



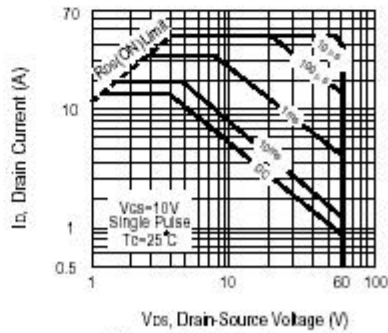
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

# CED4060AL/CEU4060AL

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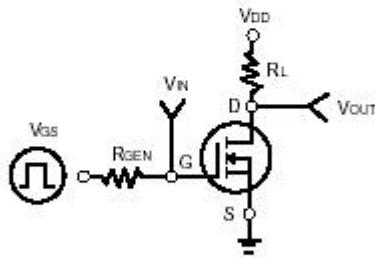


Figure 11. Switching Test Circuit

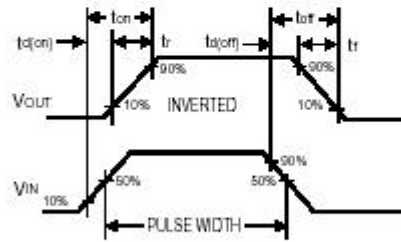


Figure 12. Switching Waveforms

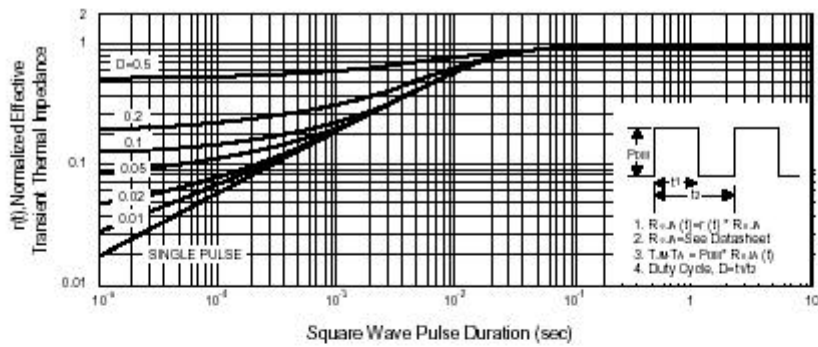


Figure 13. Normalized Thermal Transient Impedance Curve

