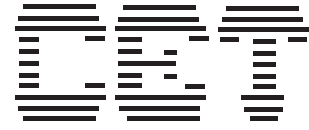


# CEF10N6



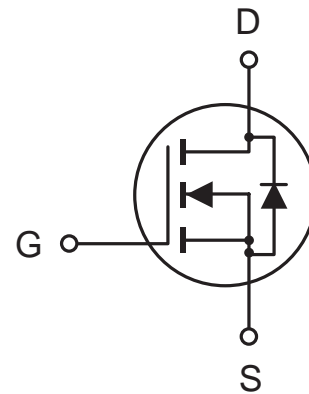
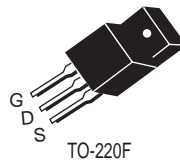
PRELIMINARY

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

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- 600V , 5.7A ,  $R_{DS(ON)}=1\Omega$  @ $V_{GS}=10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220F full-pak for through hole



### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	600	V
Gate-Source Voltage	V <sub>GS</sub>	± 30	V
Drain Current-Continuous -Pulsed	I <sub>D</sub>	5.7	A
	I <sub>DM</sub>	17	A
Drain-Source Diode Forward Current	I <sub>S</sub>	5.7	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above $25^\circ\text{C}$	P <sub>D</sub>	50	W
		0.4	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R $\theta$ JC	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R $\theta$ JA	65	°C/W

# CEF10N6

## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE AVALANCHE RATING<sup>a</sup></b>						
Single Pulse Drain-Source Avalanche Energy	E <sub>AS</sub>	V <sub>DD</sub> =50V, L=11.8mH R <sub>G</sub> =25Ω		500		mJ
Maximum Drain-Source Avalanche Current	I <sub>AS</sub>			10		A
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	600			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V			100	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2		4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> = 5A		0.75	1.0	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	10			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 40V, I <sub>D</sub> = 5A		9		S
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =300V, I <sub>D</sub> = 10A, V <sub>GS</sub> = 10V R <sub>GEN</sub> =25Ω		35	70	ns
Rise Time	t <sub>r</sub>			90	170	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			170	255	ns
Fall Time	t <sub>f</sub>			120	180	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, I <sub>D</sub> = 10A, V <sub>GS</sub> =10V		55	70	nC
Gate-Source Charge	Q <sub>gs</sub>			9		nC
Gate-Drain Charge	Q <sub>gd</sub>			22		nC

# CEF10N6

## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$		1500		pF
Output Capacitance	$C_{oss}$			125		pF
Reverse Transfer Capacitance	$C_{rss}$			50		pF
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_S=10\text{A}$			1.6	V

### Notes

a. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

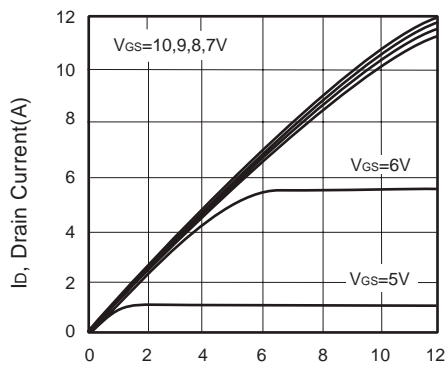


Figure 1. Output Characteristics

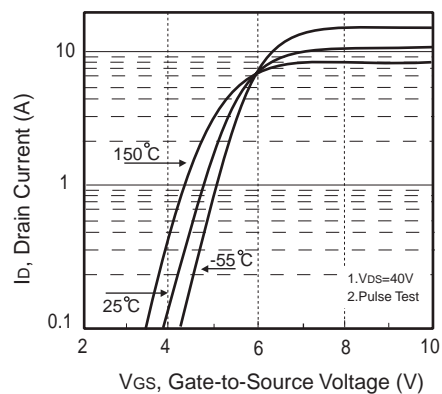
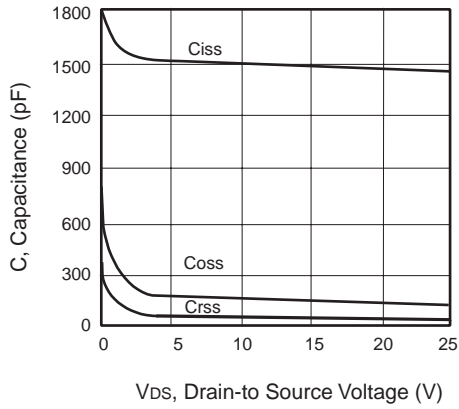


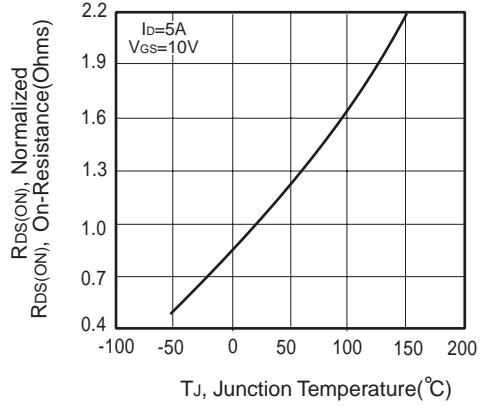
Figure 2. Transfer Characteristics

# CEF10N6

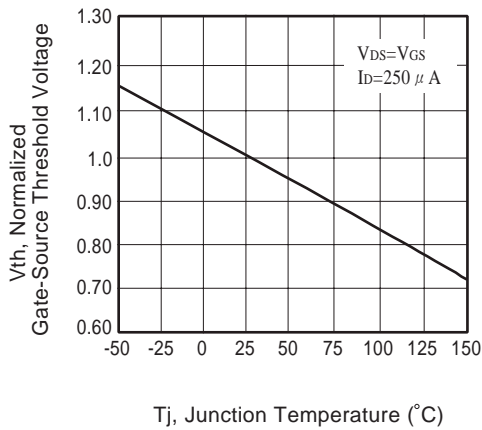
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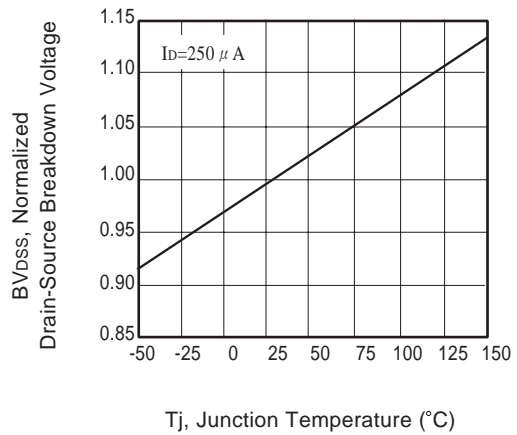
**Figure 3. Capacitance**



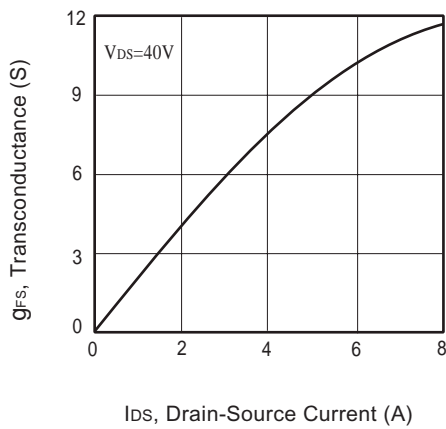
**Figure 4. On-Resistance Variation with Temperature**



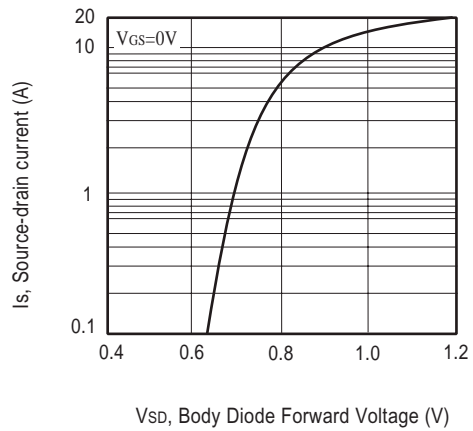
**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Breakdown Voltage Variation with Temperature**



**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**

# CEF10N6

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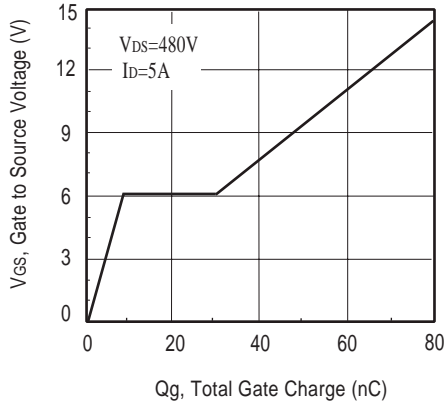


Figure 9. Gate Charge

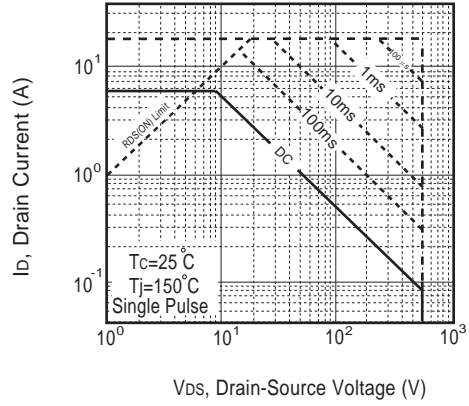


Figure 10. Maximum Safe Operating Area

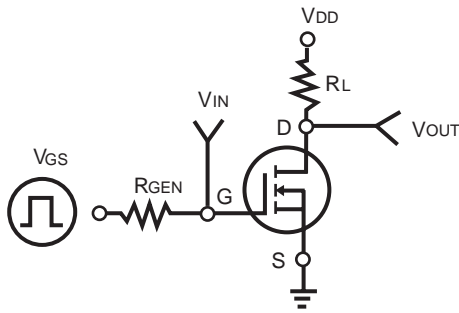


Figure 11. Switching Test Circuit

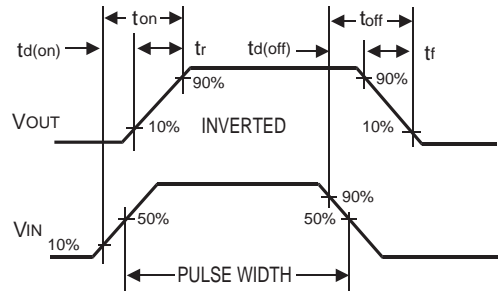


Figure 12. Switching Waveforms

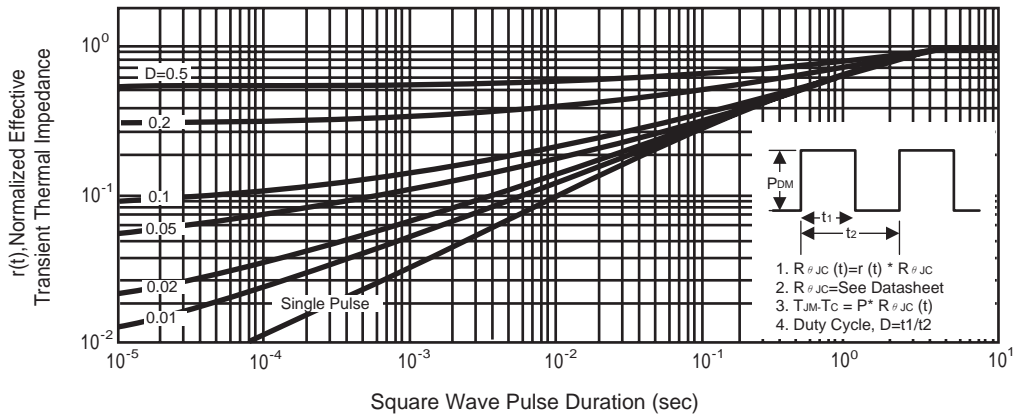


Figure 13. Normalized Thermal Transient Impedance Curve