

PCMCIA Power Controller

DESCRIPTION

The R5531V switches between the three VCC voltages (0V/3.3V/5.0V) and the VPP voltages (off/0V/3.3V/5.0V). If VCC pin or VPP pin may be clamped to the GND, short current limit works at 1A(Min.) for VCC and 0.2A(Min.) for VPP.

The R5531V is suitable for standard PCMCIA power controllers.

FEATURES

- Low on resistance P-channel MOSFET Switch
- Over- Current Limit Protection
- Thermal Shutdown Protection
- Built-in Open-drain Flag Pin
- Low Consumption Current
- Break-Before-Make Switching
- SSOP-28 pin Package

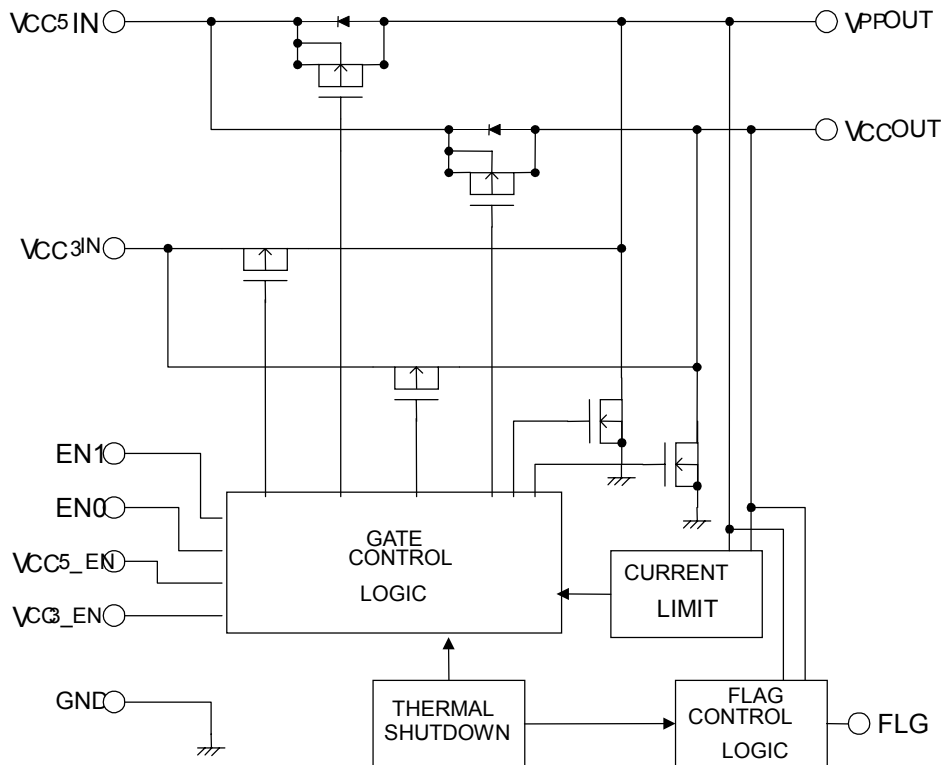
APPLICATIONS

- PC card Power Supply Pin Voltage Switch
- Card-bus Slot Power Supply Control
- PC Card Reader/Writer

PIN CONFIGURATION

VCC 5_EN	1	16	GND
VCC 3_EN	2	15	VCC5 IN
EN0	3	14	VCC OUT
EN1	4	13	VCC5 IN
FLG	5	12	VCCOUT
NC	6	11	VCC3 IN
NC	7	10	NC
VPPOUT	8	9	VCCOUT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

$T_{opt}=25^{\circ}\text{C}$

Item	Symbol	Conditions	Ratings	Unit
Input Voltage(5V)	V_{cc5}		-0.3 to 6.0	V
Input Voltage(3V)	V_{cc3}		-0.3 to 6.0	V
Flag Voltage	V_{FLG}		-0.3 to 6.0	V
Logic Input Voltage	V_{IN}		-0.3 to 6.0	V
Operating Temperature Range	T_{opt}		-40 to 85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}		-55 to 125	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

TopT=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V _{cc5}	Supply Voltage(5V)		3.0	5.0	5.5	V
V _{cc3}	Supply Voltage(3V)		3.0	3.3	5.5	V
I _{cc5}	Supply Current(each slot)	V _{cc} OUT = 5V or 3.3V		30	60	μA
I _{SLP5}		V _{cc} OUT = 0V (sleep mode)		0.2	10.0	μA
I _{CC3}		V _{cc} OUT = 5V or 3.3V		10	30	μA
I _{SLP3}		V _{cc} OUT = 0V (sleep mode)		0.1	10	μA
RoV _{cc}	V _{cc} OUT switch resistance	Select V _{cc} OUT=5V		85	140	mΩ
		Select V _{cc} OUT=3.3V		100	150	mΩ
		Select V _{cc} OUT=0V		500	3900	Ω
RoV _{pp}	V _{pp} OUT switch resistance	Select V _{pp} OUT=5V		1.8	2.5	Ω
		Select V _{pp} OUT=3.3V		3.3	5.0	Ω
		Select V _{pp} OUT=0V		2500	3900	Ω
IPPL	V _{pp} OUT Leakage Current	Select V _{pp} OUT=Hi-Z		1	10	μA
ICCSC	Short Current Limit	V _{cc} OUT=0V	1	1.5		A
IPpsc		V _{pp} OUT=0V	0.2	0.3		A
V _{IH}	Logic Input "H" Voltage		2.2		6.0	V
V _{IL}	Logic Input "L" Voltage		-0.3		0.8	V
I _{IN}	Logic Input Current		-1		1	μA
TSD	Thermal Shutdown Temperature			135		°C
VOOK	Flag Threshold Voltage	FLG is pulled up to V _{CC3IN} with 10kΩ		V _{cc} -1 V _{pp} -1		V
t ₁	V _{cc} Turn-on Delay Time (*Note 2)	V _{cc} OUT=0V to 10% of 3.3V		300	1500	μs
t ₂		V _{cc} OUT=0V to 10% of 5.0V		500	3000	μs
t ₃	V _{cc} Rising Time (*Note 2)	V _{cc} OUT=10% to 90% of 3.3V	200	800	2500	μs
t ₄		V _{cc} OUT=10% to 90% of 5.0V	200	1800	6000	μs
t ₇	V _{cc} Turn-off Delay Time (*Note1,2,4)	V _{cc} OUT=3.3V to Hi-Z		2.3	8.0	ms
t ₈		V _{cc} OUT=5V to Hi-Z		2.8	8.0	ms
t ₅	V _{cc} Falling Time (*Note 3)	V _{cc} OUT=90% to 10% of 3.3V	100	700	1500	μs
t ₆		V _{cc} OUT=90% to 10% of 5.0V	100	600	2000	μs
t ₉	V _{pp} Turn-on Delay Time (*Note 3)	V _{pp} OUT=0V to 10% of 3.3V		15	50	μs
t ₁₀		V _{pp} OUT=0V to 10% of 5.0V		25	50	μs
t ₁₁	V _{pp} Rising Time (*Note 3)	V _{pp} OUT=10% to 90% of 3.3V	100	200	800	μs
t ₁₂		V _{pp} OUT=10% to 90% of 5.0V	100	280	1000	μs
t ₁₅	V _{pp} Turn-off Delay Time (*Note 1,3)	V _{pp} OUT=3.3V to Hi-Z		0.1	1.0	μs
t ₁₆		V _{pp} OUT=5V to Hi-Z		0.1	1.0	μs
t ₁₃	V _{pp} Falling Time (*Note 3)	V _{pp} OUT=90% to 10% of 3.3V		0.05	1.00	μs
t ₁₄		V _{pp} OUT=90% to 10% of 5.0V		0.05	1.00	μs

(*Note1) Delay from commanding Hi-Z or 0V to beginning slope

(*Note2) t₁ to t₈ Test Condition: RL=10Ω

(*Note3) t₉ to t₁₅ Test Condition: RL=100Ω

(*Note4) Do not apply to current limit or thermal shutdown conditions during these terms

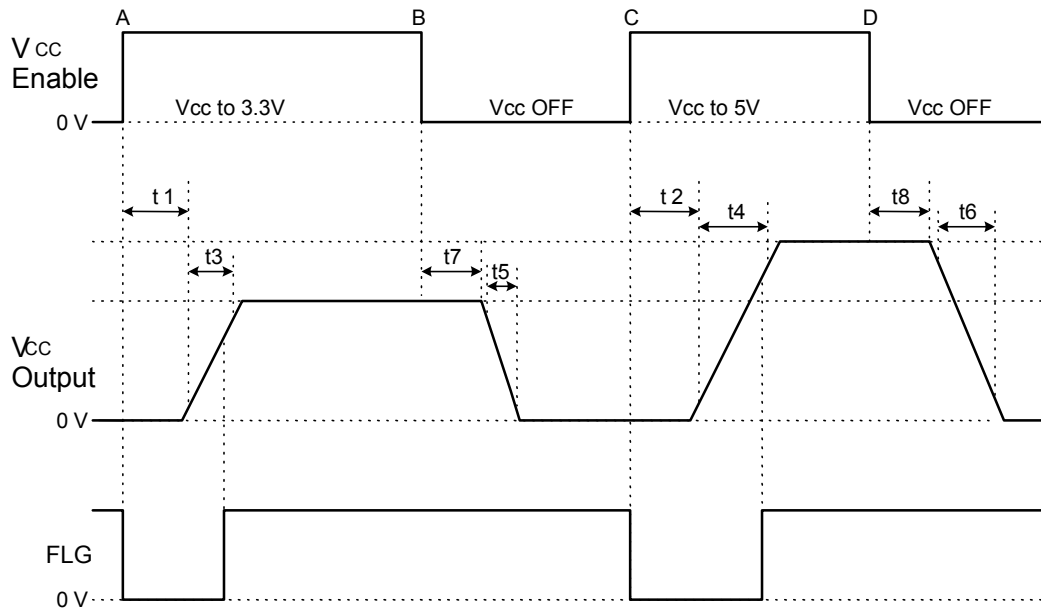


Fig.1 R5531V V_{CC} Timing Diagram

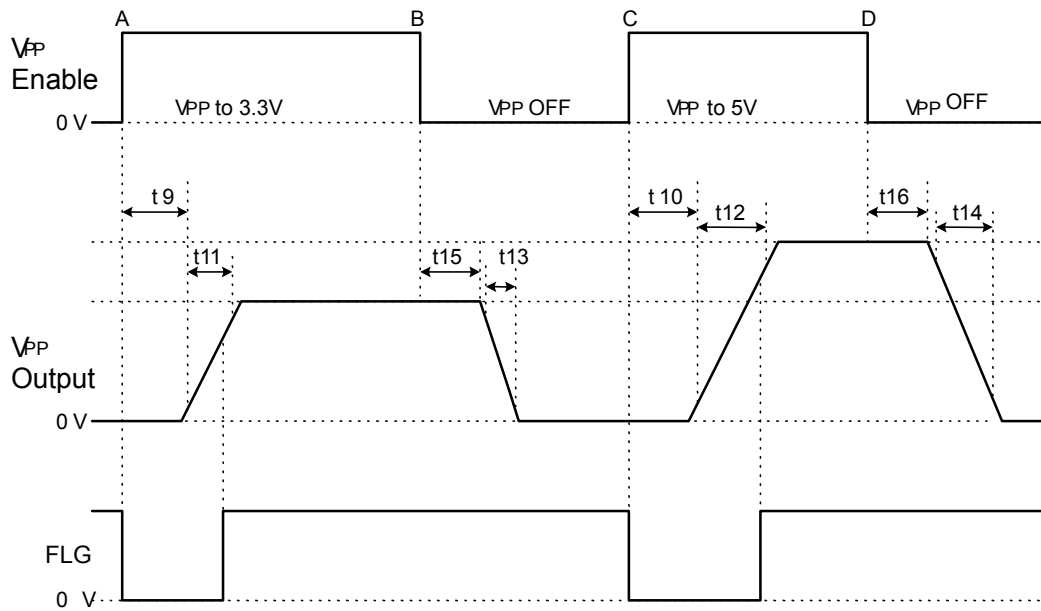


Fig. 2 R5531V V_{PP} Timing Diagram

R5531V001 Control Logic Table

Vcc5_EN	Vcc3_EN	EN1	EN0	Vcc OUT	Vpp OUT
0	0	0	0	0V	Hi-Z
0	0	0	1	0V	Hi-Z
0	0	1	0	0V	Hi-Z
0	0	1	1	0V	0V
0	1	0	0	3.3V	Hi-Z
0	1	0	1	3.3V	3.3V
0	1	1	0	3.3V	Hi-Z
0	1	1	1	3.3V	0V
1	0	0	0	5.0V	Hi-Z
1	0	0	1	5.0V	5V
1	0	1	0	5.0V	Hi-Z
1	0	1	1	5.0V	0V
1	1	0	0	3.3V	Hi-Z
1	1	0	1	3.3V	3.3V
1	1	1	0	3.3V	5V
1	1	1	1	3.3V	0V

R5531V002 Control Logic Table

Vcc5_EN	Vcc3_EN	EN1	EN0	Vcc OUT	Vpp OUT
0	0	0	0	0V	0V
0	0	0	1	0V	Hi-Z
0	0	1	0	0V	Hi-Z
0	0	1	1	0V	Hi-Z
0	1	0	0	5V	0V
0	1	0	1	5V	5V
0	1	1	0	5V	Hi-Z
0	1	1	1	5V	Hi-Z
1	0	0	0	3.3V	0V
1	0	0	1	3.3V	3.3V
1	0	1	0	3.3V	Hi-Z
1	0	1	1	3.3V	Hi-Z
1	1	0	0	0V	0V
1	1	0	1	0V	Hi-Z
1	1	1	0	0V	Hi-Z
1	1	1	1	0V	Hi-Z

■APPLICATION NOTES

- * VCC5IN voltage should be equal or more than VCC3IN.
- * Same name pins should be connected one another.
- * There is a parasitic diode between source and drain of the switch transistors. (Refer to the block diagram.) Therefore, even if the switch may be disabled, in case the OUT voltage is higher than VCC5IN, some current flows from OUT to VCC5IN.