QUALITY POLICY

To achieve customer satisfaction and improve our business
through quality, we are committed to:

1. Knowing customer’ s expectations and needs, continually providing high quality products.

2. Solving customer complaints immediately, preventing problems from recurring and occurring, and earning customer trust.

3. Developing a quality management system and making consistent improvements of its effectiveness

4. Setting quality goals from a customer’ s viewpoint, understanding the condition of achievement and reviewing the appropriateness and adequateness of the goals.

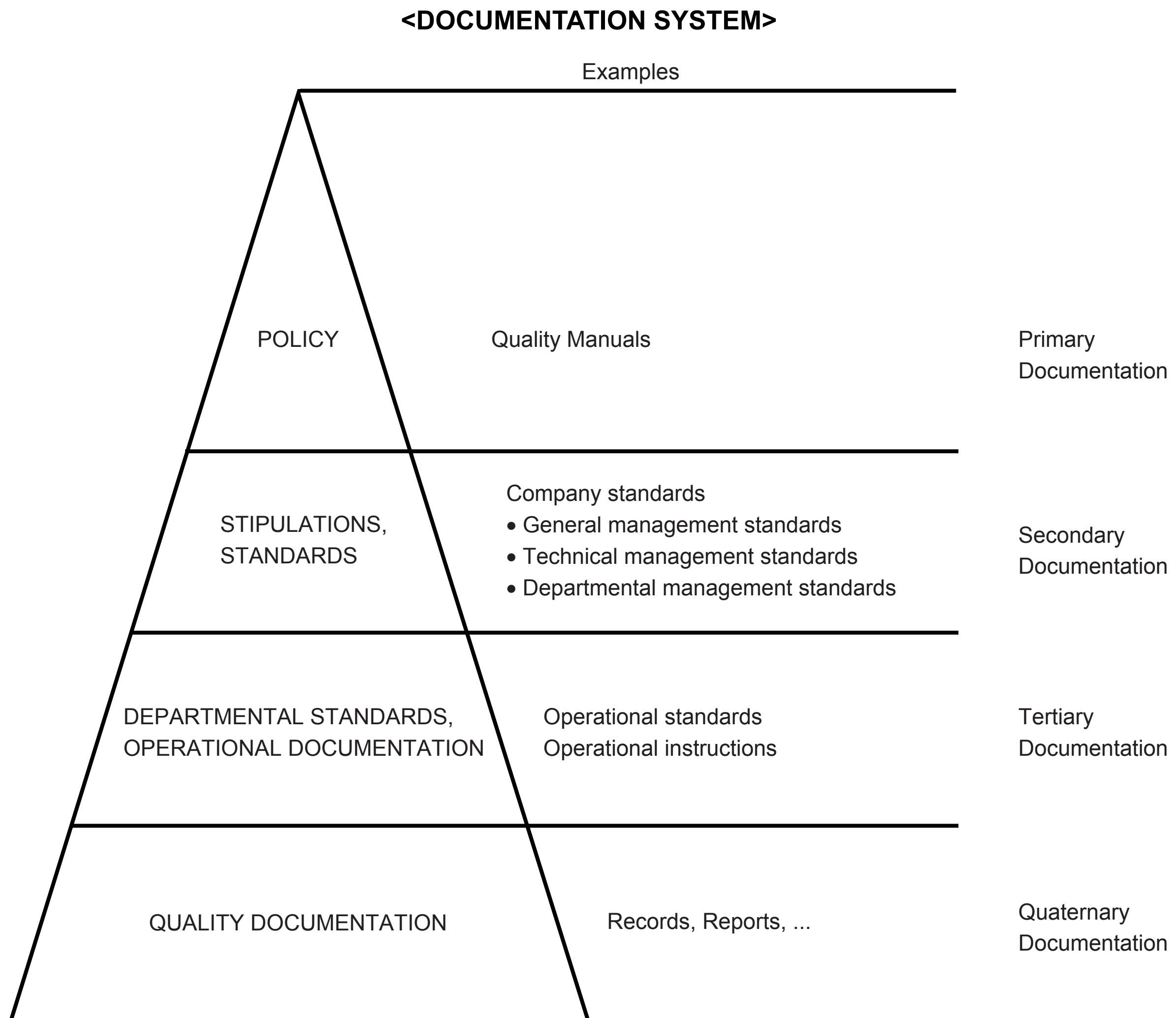
QUALITY SYSTEM

In order to ensure that a product conforms to stipulated requirements, a Quality System has been established. The Quality System is communicated to all concerned personnel in this Company.

1. Quality Manual has been established to ensure implementation of the Quality System based on the requirements of the ISO9001(2000).

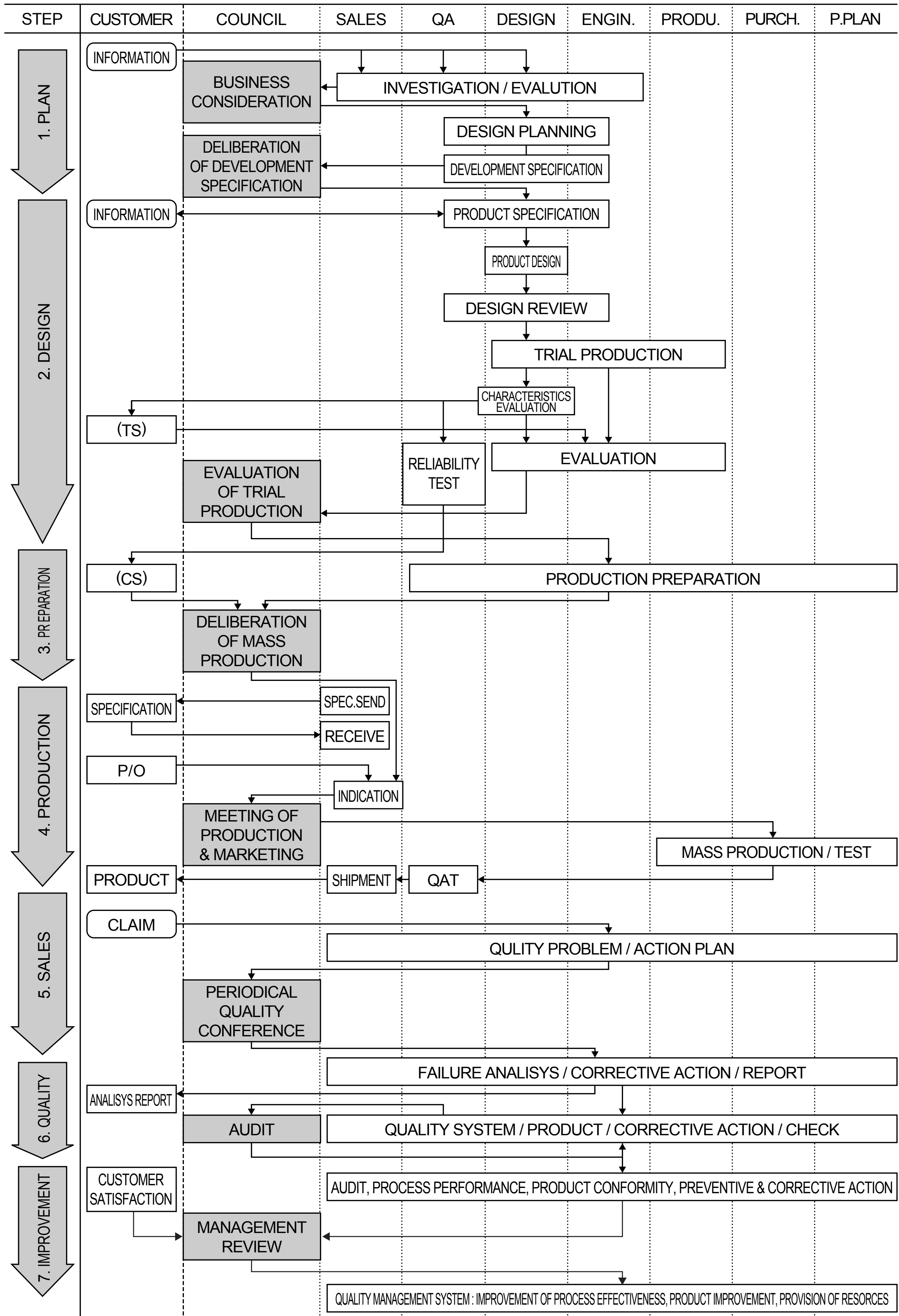
2. Written standards and procedures for efficiently implementing the Quality System and meeting stipulated requirements have been established. The details of these written documents vary depending on job complexity, method, technique, and training.

<DOCUMENTATION SYSTEM>

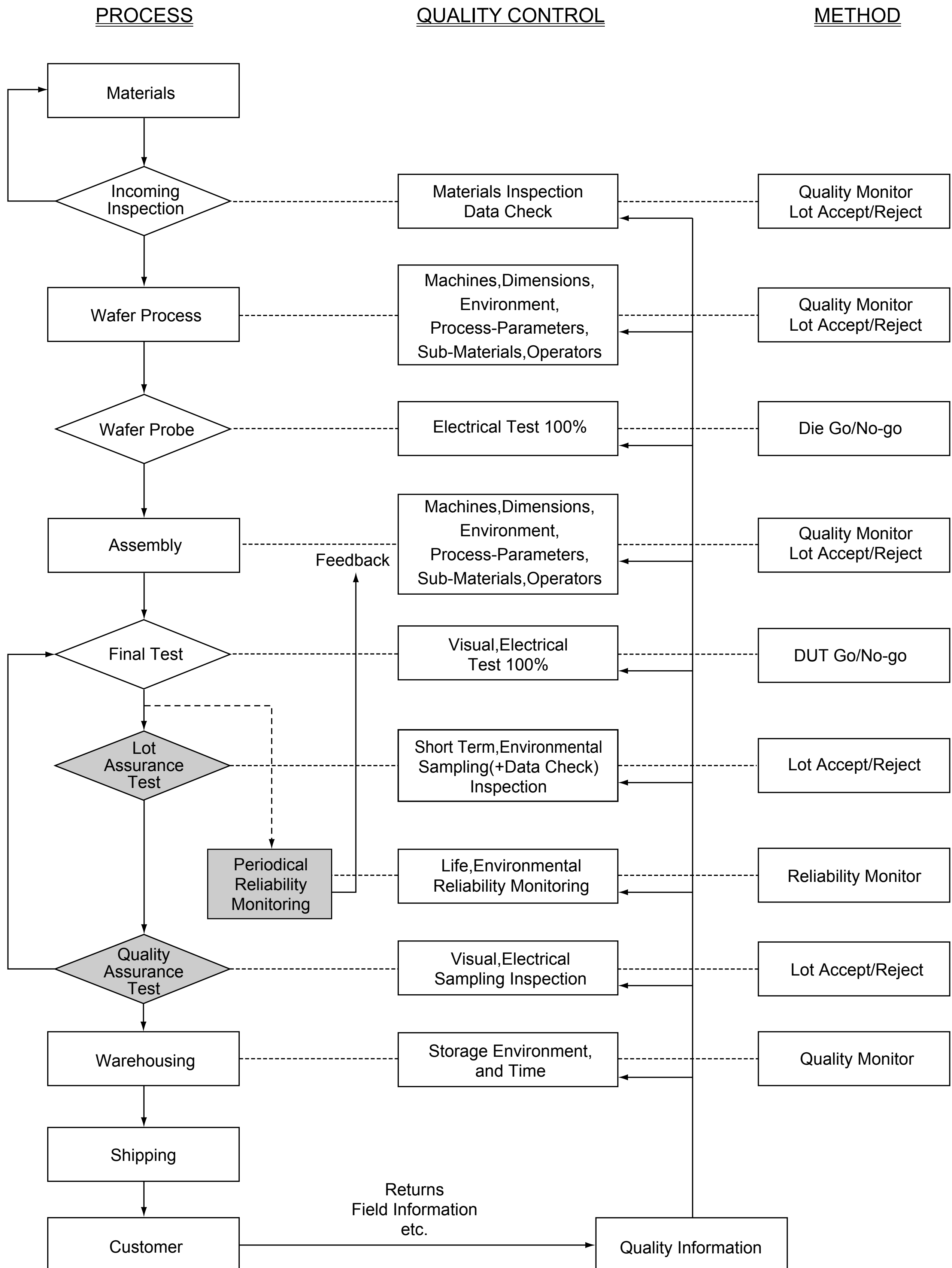


QUALITY ASSURANCE SYSTEM

(for Power Management ICs)



QUALITY CONTROL FLOW CHART



LOT ASSURANCE INSPECTION

LOT ASSURANCE INSPECTION is executed to verify the quality every wafer process fabrication lot. It is the key to the assured delivery initial reliability.

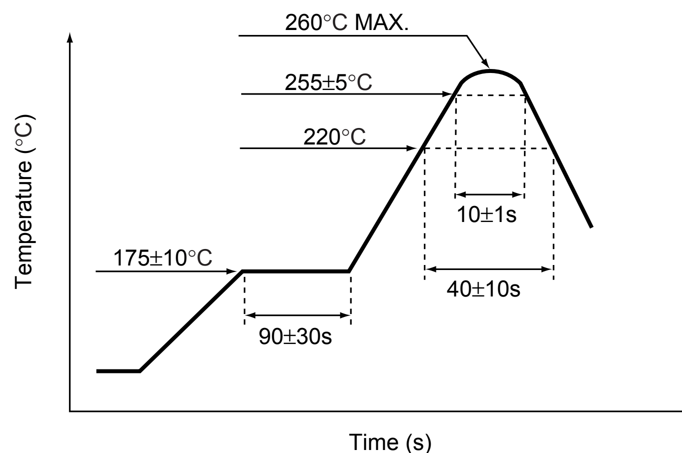
(for Power Management ICs)

<table>
<tr><th>No.</th><th colspan="2">TEST ITEMS</th><th>TEST CONDITION</th><th>Sample</th><th>LTPD</th></tr>
<tr><td>1</td><td colspan="2">High Temperature
Operating Test</td><td>Ta=125°C
48h</td><td>22</td><td>10%</td></tr>
<tr><td rowspan="3">2</td><td rowspan="2">Heat
Treatment</td><td>Soldering Heat
(TO-92 Package)</td><td>Ta=260°C 10s
Immersion in Solder Bath</td><td rowspan="3">22</td><td rowspan="3">10%</td></tr>
<tr><td>IR Reflow
(SMD Package)</td><td>Heating Profile (Fig-1) Twice</td></tr>
<tr><td colspan="2">Pressure Cooker Bias Test
(USPCBT)</td><td>Ta=125°C
RH=85%
20h</td></tr>
</table>

<Inspection Period>

Basically, LOT ASSURANCE INSPECTION is implemented in each shipping lot. After the quality level is stabilized, the inspection will shift to the periodical monitoring.

Fig-1 HEATING TREATMENT CONDITION OF INFRARED-RAY REFLOW



QUALITY ASSURANCE TEST INSPECTION

QUALITY ASSURANCE TEST INSPECTION is a sampling type inspection for finally verifying the delivery initial quality (electrical, visual) of a product to be delivered.

(for Power Management ICs)

DIVISION	TEST ITEMS	CRITERIA	LEVEL*2
Electrical	Heavy Defect	QAT Specification	AQL 0.065%*1
	Light Defect		AQL 0.15%
Appearance	Heavy Defect	Visual Inspection Criteria	AQL 0.25%
	Light Defect		AQL 0.65%

*1) Catastrophic Failures (short, open or functionally inoperative) AQL 0.065%
*2) AQL : ANSI/ASQC Z1.4-1993
Sampling Plans : Table Ⅱ-C-Single sampling plans for reduced inspection

PERIODICAL RELIABILITY MONITORING

PERIODICAL RELIABILITY MONITORING is executed to verify that the long-term reliability is retained at the same level after the product is authorized and to verify the stabilized quality and reliability of a wafer process or assembly process.

A period of time is specified for each type of circuit function or process technique to execute life and environmental tests. Information and data gained are feed back to the fabrication process and stored to retain or improve the reliability.

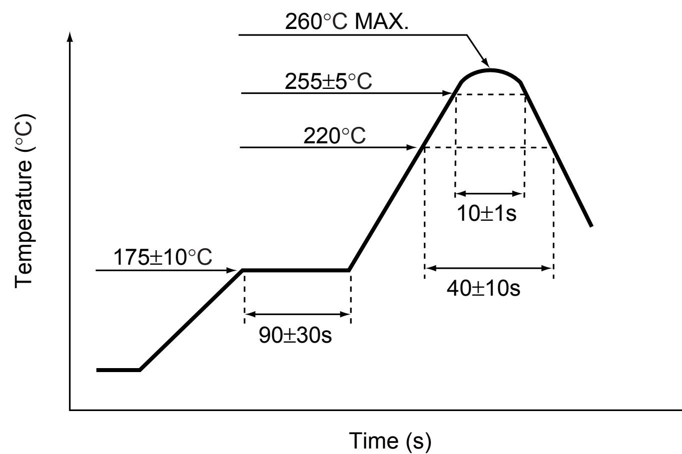
(for Power Management ICs)

No.	TEST ITEMS	TEST CONDITION	Sample SIZE	Sample	PERIOD
1	High Temperature Operating Life	Ta=125°C DC 1000h	22	At least 1item / process /package	Every 6month
2	High Temperature Storage	Ta=150°C 1000h	22		
3	Temperature Cycle	Ta=-65 to 150°C 100cycles	22		
4	Pressure Cooker Bias (USPCBT)	Ta=125°C RH=85% DC 100h	22		

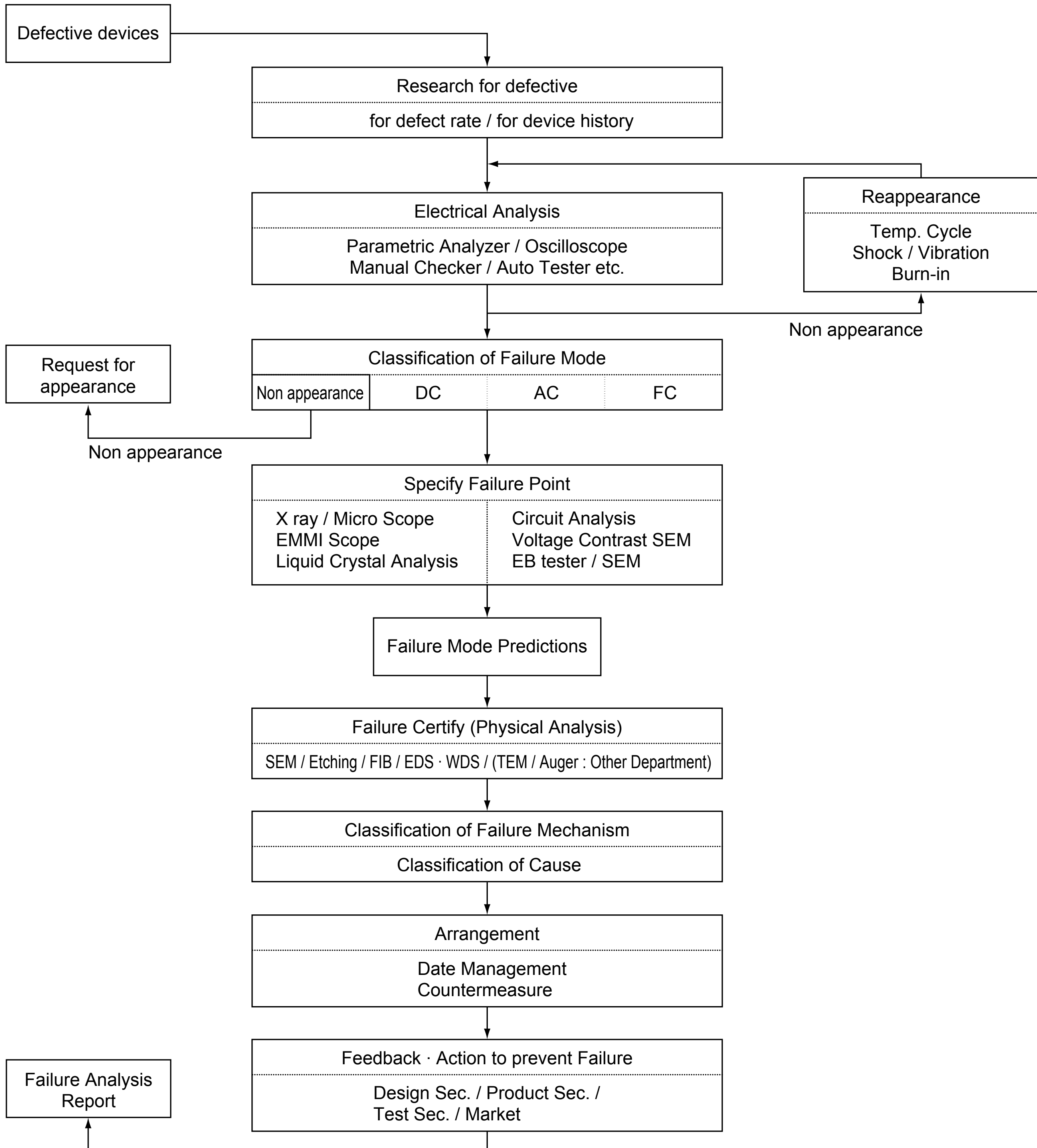
Pre-condition : [SMD] 85°C 85%RH 168h + IR Reflow (Fig-1) 3times

[DIP] 85°C 85%RH 168h + Solder Dipping (260°C 10s) Once

Fig-1 HEATING TREATMENT CONDITION OF INFRARED-RAY REFLOW



FAILURE ANALYSIS FLOW CHART



RELIABILITY TEST REQUIREMENTS

(for SOT89, SOT89-5 Package)

No.	TEST ITEMS	TEST CONDITIONS	DURATION	SAMPLE SIZE	ACCEPT/ REJECT
1	High Temperature Operating Bias Test	Ta=125°C DC=V_{DD} (Max.)	1000h	32	0/1
2	Temperature and Humidity Bias Test	Ta=60°C RH=90% DC=V_{DD} (Max.)	1000h	22	0/1
3	High Temperature Storage Test	Ta=150°C	1000h	22	0/1
4	Low Temperature Storage Test	Ta=-65°C	1000h	22	0/1
5	Temperature and Humidity Storage Test	Ta=85°C RH=85%	1000h	22	0/1
6	Temperature Cycling Test (air)	Ta=-65 to 150°C (30-5-30min)	100cycles	11	0/1
7	Thermal Shock Test (Liquid)	Ta=-65 to 150°C (5min-10s-5min)	100cycles	11	0/1
8	USPCBT	Ta=125°C RH=85% 2×10^5Pa DC=V_{DD} (Max.)	100h	11	0/1
9	USPCT	Ta=125°C RH=85% 2×10^5Pa	100h	11	0/1
10	Resistance to soldering heat	Ta=85°C RH=85% t=168h — IR Reflow (see Fig-1)	3times	11	0/1
		Ta=350°C (only terminal)	5s	11	0/1
11	Solderability	Ta=235°C (4h aging in steam)	5s	11	0/1
12	ESD Sensitivity (1)	C=200pF R=0Ω ±150V (Min.)	5times	11	0/1
	ESD Sensitivity (2)	C=100pF R=1.5kΩ ±1kV (Min.)	3times	11	0/1
13	Latch Up	Pulse Current Injecting Method ±100mA (Min.)	once	11	0/1

[Pre-condition]

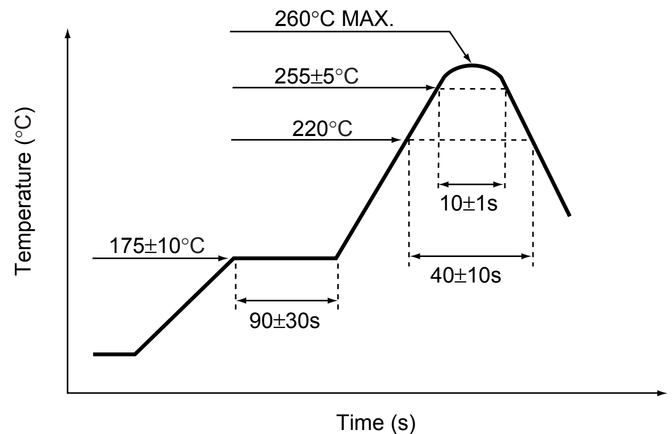
Test No.2, 5 to 9 shall be performed this pre-condition before testing.

- Ta=85°C RH=85% Storage 168h

  ↓

- IR Reflow soldering heat stress (3times)

Fig-1 HEATING TREATMENT CONDITION OF INFRARED-RAY REFLOW



RELIABILITY TEST REQUIREMENTS

(for SC82AB, SOT23, SON Package)

No.	TEST ITEMS	TEST CONDITIONS	DURATION	SAMPLE SIZE	ACCEPT/ REJECT
1	High Temperature Operating Bias Test	Ta=125°C DC=V_{DD} (Max.)	1000h	32	0/1
2	Temperature and Humidity Bias Test	Ta=85°C RH=85% DC=V_{DD} (Max.)	1000h	22	0/1
3	High Temperature Storage Test	Ta=150°C	1000h	22	0/1
4	Low Temperature Storage Test	Ta=-65°C	1000h	22	0/1
5	Temperature and Humidity Storage Test	Ta=85°C RH=85%	1000h	22	0/1
6	Temperature Cycling Test (air)	Ta=-65 to 150°C (30-5-30min)	100cycles	11	0/1
7	Thermal Shock Test (Liquid)	Ta=-65 to 150°C (5min-10s-5min)	100cycles	11	0/1
8	USPCBT	Ta=125°C RH=85% 2×10^5Pa DC=V_{DD} (Max.)	100h	11	0/1
9	USPCT	Ta=125°C RH=85% 2×10^5Pa	100h	11	0/1
10	Resistance to soldering heat	Ta=85°C RH=85% t=168h: IR Reflow (see Fig-1)	3times	11	0/1
		Ta=85°C RH=85% t=168h: Ta=350°C (only terminal)	5s	11	0/1
11	Solderability	Ta=235°C (4h aging in steam)	5s	11	0/1
12	ESD Sensitivity (1)	C=200pF R=0Ω ±150V (Min.)	5times	11	0/1
	ESD Sensitivity (2)	C=100pF R=1.5kΩ ±1kV (Min.)	3times	11	0/1
13	Latch Up	Pulse Current Injecting Method ±100mA (Min.)	once	11	0/1

[Pre-condition]

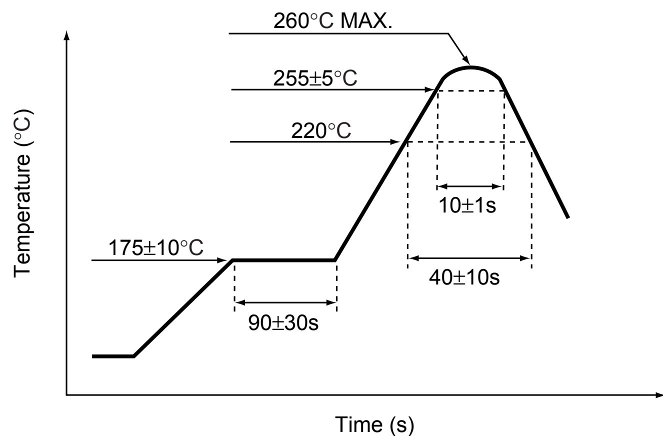
Test No.2, 5 to 9 shall be performed this pre-condition before testing.

- Ta=85°C RH=85% Storage 168h

  ↓

- IR Reflow soldering heat stress (3times)

Fig-1 HEATING TREATMENT CONDITION OF INFRARED-RAY REFLOW



RELIABILITY TEST REQUIREMENTS

(for SOP, SSOP Package)

No.	TEST ITEMS	TEST CONDITIONS	DURATION	SAMPLE SIZE	ACCEPT/ REJECT
1	High Temperature Operating Bias Test	Ta=125°C DC=V_{DD} (Max.)	1000h	32	0/1
2	Temperature and Humidity Bias Test	Ta=85°C RH=85% DC=V_{DD} (Max.)	1000h	22	0/1
3	High Temperature Storage Test	Ta=125°C	1000h	22	0/1
4	Low Temperature Storage Test	Ta=-55°C	1000h	22	0/1
5	Temperature and Humidity Storage Test	Ta=85°C RH=85%	1000h	22	0/1
6	Temperature Cycling Test (air)	Ta=-55 to 125°C (30-5-30min)	100cycles	11	0/1
7	Thermal Shock Test (Liquid)	Ta=-55 to 125°C (5min-10s-5min)	100cycles	11	0/1
8	USPCBT	Ta=125°C RH=85% 2×10^5Pa DC=V_{DD} (Max.)	100h	11	0/1
9	USPCT	Ta=125°C RH=85% 2×10^5Pa	100h	11	0/1
10	Resistance to soldering heat	Ta=85°C RH=85% t=168h / IR Reflow (see Fig-1)	3times	11	0/1
		Ta=85°C RH=85% t=168h / Ta=350°C (only terminal)	5s	11	0/1
11	Solderability	Ta=235°C (4h aging in steam)	5s	11	0/1
12	ESD Sensitivity (1)	C=200pF R=0Ω ±150V (Min.)	5times	11	0/1
	ESD Sensitivity (2)	C=100pF R=1.5kΩ ±1kV (Min.)	3times	11	0/1
13	Latch Up	Pulse Current Injecting Method ±100mA（Min.）	once	11	0/1

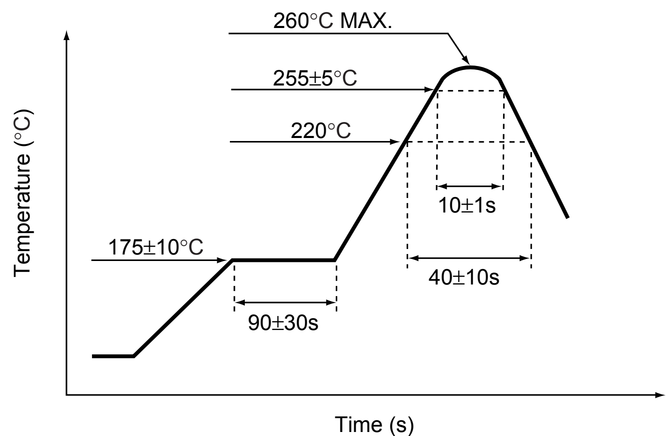
[Pre-condition]
Test No.2, 5 to 9 shall be performed this pre-condition before testing.

- Ta=85°C RH=85% Storage 168h

  ↓

- IR Reflow soldering heat stress (3times)

Fig-1 HEATING TREATMENT CONDITION OF INFRARED-RAY REFLOW



RELIABILITY TEST REQUIREMENTS

(for TO-92 Package)

<table>
<tr><th>No.</th><th>TEST ITEMS</th><th colspan="2">TEST CONDITIONS</th><th>DURATION</th><th>SAMPLE SIZE</th><th>ACCEPT/ REJECT</th></tr>
<tr><td>1</td><td>High Temperature Operating Bias Test</td><td colspan="2">Ta=125°C DC=V_{DD} (Max.)</td><td>1000h</td><td>32</td><td>0/1</td></tr>
<tr><td>2</td><td>Temperature and Humidity Bias Test</td><td colspan="2">Ta=85°C RH=85% DC=V_{DD} (Max.)</td><td>1000h</td><td>22</td><td>0/1</td></tr>
<tr><td>3</td><td>High Temperature Storage Test</td><td colspan="2">Ta=150°C</td><td>1000h</td><td>22</td><td>0/1</td></tr>
<tr><td>4</td><td>Low Temperature Storage Test</td><td colspan="2">Ta=-65°C</td><td>1000h</td><td>22</td><td>0/1</td></tr>
<tr><td>5</td><td>Temperature and Humidity Storage Test</td><td colspan="2">Ta=85°C RH=85%</td><td>1000h</td><td>22</td><td>0/1</td></tr>
<tr><td>6</td><td>Temperature Cycling Test (air)</td><td colspan="2">Ta=-65 to 150°C (30-5-30min)</td><td>100cycles</td><td>11</td><td>0/1</td></tr>
<tr><td>7</td><td>Thermal Shock Test (Liquid)</td><td colspan="2">Ta=-65 to 150°C (5min-10s-5min)</td><td>100cycles</td><td>11</td><td>0/1</td></tr>
<tr><td>8</td><td>USPCBT</td><td colspan="2">Ta=125°C RH=85% 2×10^5Pa DC=V_{DD} (Max.)</td><td>100h</td><td>11</td><td>0/1</td></tr>
<tr><td>9</td><td>USPCT</td><td colspan="2">Ta=125°C RH=85% 2×10^5Pa</td><td>100h</td><td>11</td><td>0/1</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">Resistance to soldering heat</td><td rowspan="2">Ta=85°C
RH=85%
t=168h</td><td>Ta=260°C (only terminal)</td><td>10s</td><td>11</td><td>0/1</td></tr>
<tr><td>Ta=350°C (only terminal)</td><td>5s</td><td>11</td><td>0/1</td></tr>
<tr><td>11</td><td>Solderability</td><td colspan="2">Ta=235°C (4h aging in steam)</td><td>5s</td><td>11</td><td>0/1</td></tr>
<tr><td rowspan="2">12</td><td>ESD Sensitivity (1)</td><td colspan="2">C=200pF R=0Ω ±150V (Min.)</td><td>5times</td><td>11</td><td>0/1</td></tr>
<tr><td>ESD Sensitivity (2)</td><td colspan="2">C=100pF R=1.5kΩ ±1kV (Min.)</td><td>3times</td><td>11</td><td>0/1</td></tr>
<tr><td>13</td><td>Latch Up</td><td colspan="2">Pulse Current Injecting Method ±100mA（Min.）</td><td>once</td><td>11</td><td>0/1</td></tr>
</table>

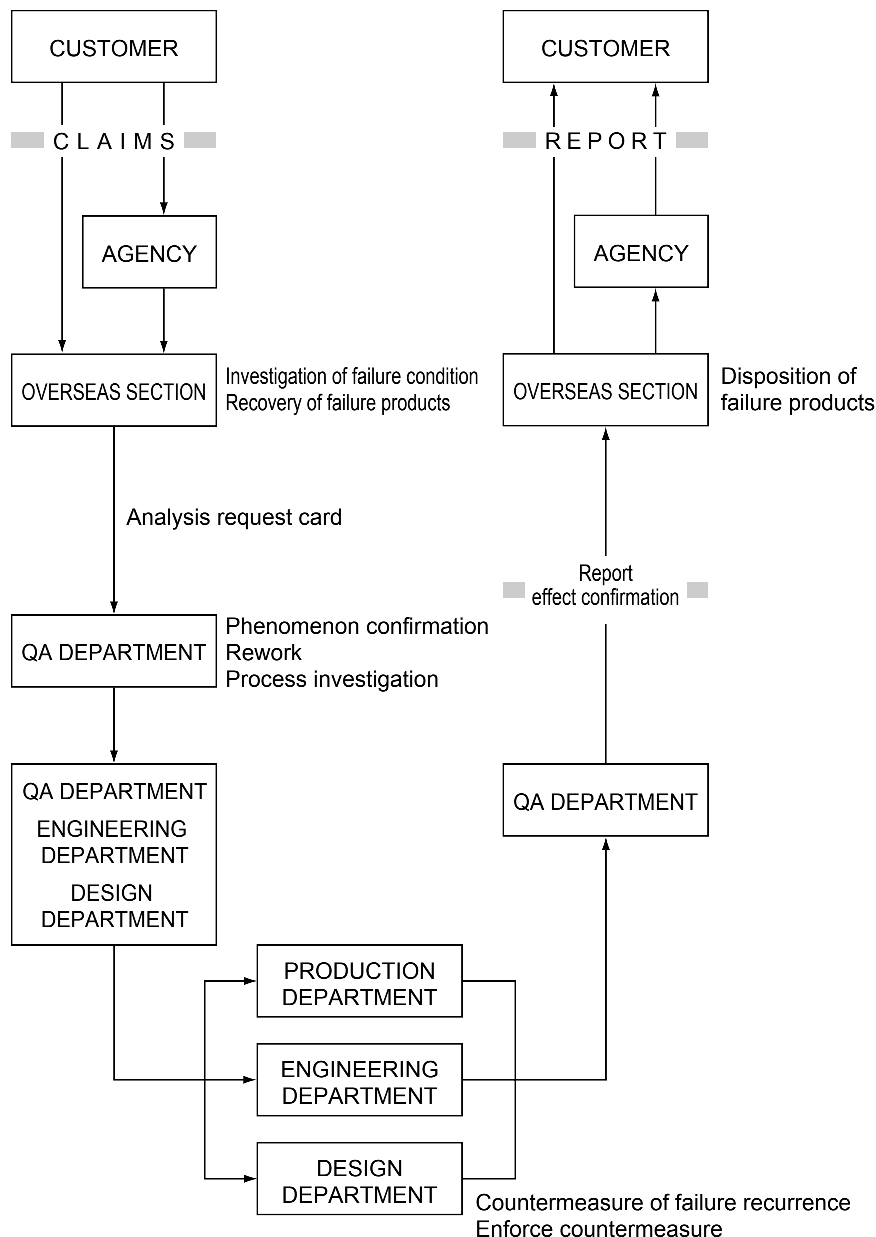
[Pre-condition]
Test No.2, 5 to 9 shall be performed this pre-condition before testing.

- Ta=85°C RH=85% Storage 168h

  ↓
- Ta=260°C 10s (Soldering heat stress)

COMPLAINT HANDLING SYSTEM

If a defective or other failure occurs in an acceptance inspection, assembly process, or the like unfortunately after the delivery of a product, our business department will take back the product in failure immediately in response to your request to minimize your failure or loss. Or, we may ask you to return it. In such cases, we investigate the usage condition and period of time prior to the failure and the condition at that time when the failure occurred. On the basis of the information, our quality assurance department makes an effort to identify the case of the failure in cooperation with our technical and design departments, while feeding back the information to the fabrication processes, to improve the quality and prevent recurrence. Interim reports or replies are sent to our customers.



HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

1. Soldering

1-1 The surface temperature and the exposure time should be kept as below.

Max. Temp.	Max. Time	Applicable part
260°C	10s	Lead
235°C	10s	Body
350°C	5s	Lead (when hand-soldering is necessary)

1-2 Don’t use halogenous solder flux.

1-3 Recommended heating profiles are shown in Fig-1 to Fig-3
Baking step preceding reflow process is not necessary. Though heating process may be carried out twice, in reflow method, be sure to minimize the temperature and the exposure time.

1-4 The board cleaning conditions.

1-4.1 We recommend alternative CFCs substitute for solvent.
ex.ST-100s (Arakawa)
Don’t use trichloroethylene, trichloroethane, etc.

1-4.2 Cleaning time should be less than 180s (including in solvent, in vapor and in ultrasonic bath).

1-4.3 Ultrasonic cleaning is usable

Frequency	28 to 40kHz (resonant damage should be avoided)
Power	15W/l (Max.)
Time	60s (Max.)

2. Storage

Please be sure to store devices in proper conditions to maintain device quality.

Ambient temperature	5 to 35°C
Humidity	45 to 75%

(Note) If humidifiers are being used, provide pure water or boiled water.
When the devices are stored in the long term, maintain the air purified and the temperature stabilized.

3. Anti E.S.D.

Relative humidity should be maintain more than 60% in the manufacturing workstation.
All parts of machines which come into contact with the ICs must be grounded metal or other conductive material.
When hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

4. Recommended Heating Profile

Fig-1: Reflow profile (Standard)

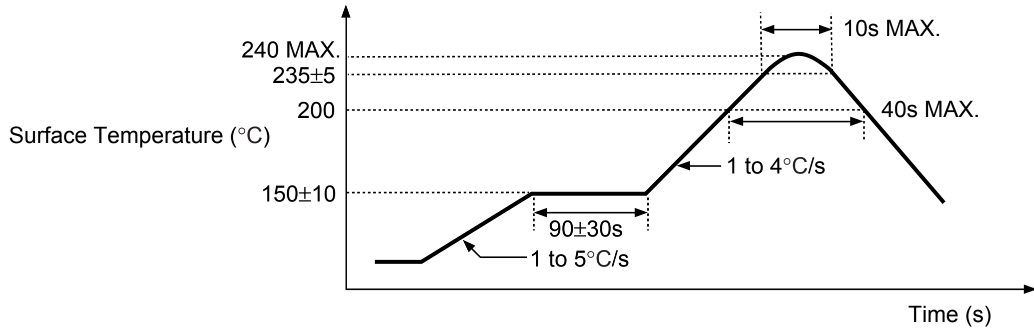


Fig-2: Reflow profile (Lead free)

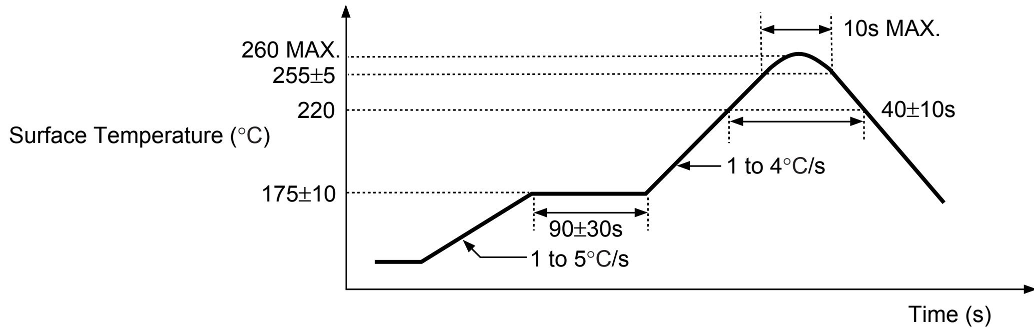
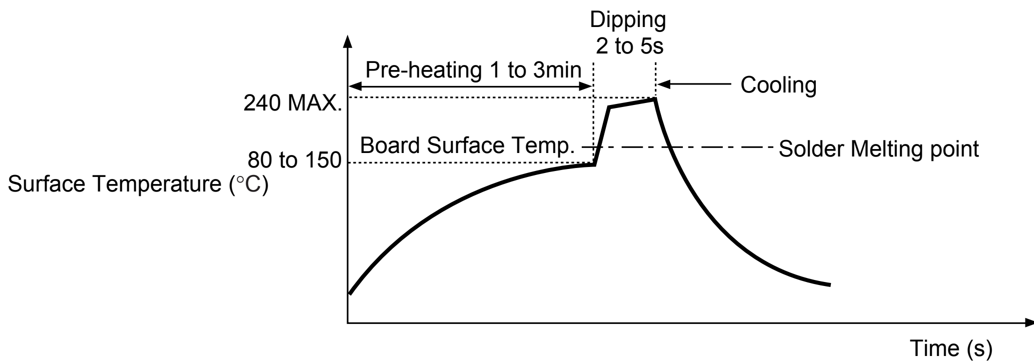
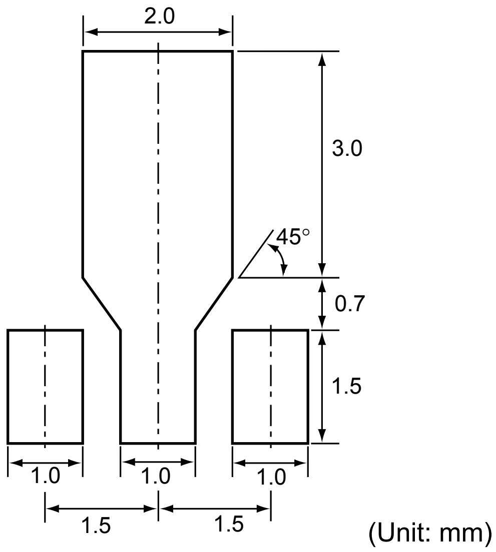


Fig-3: Dip Soldering for SOT-23/TO-92 (Reference)



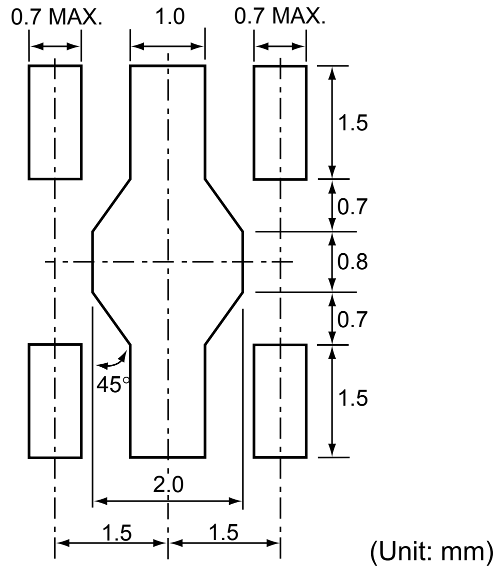
RECOMMENDED LAND PATTERN

● **SOT-89-3**



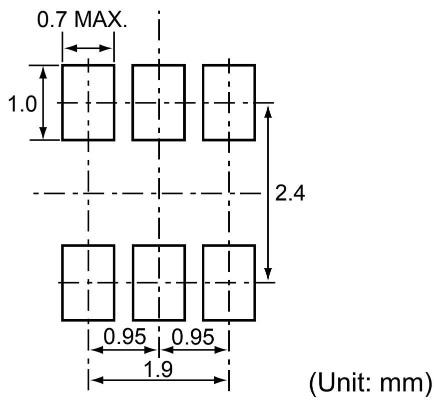
(Unit: mm)

● **SOT-89-5**



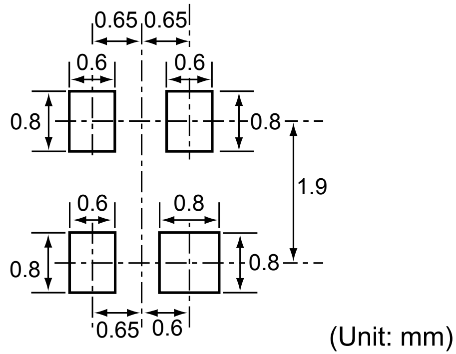
(Unit: mm)

● **SOT-23**



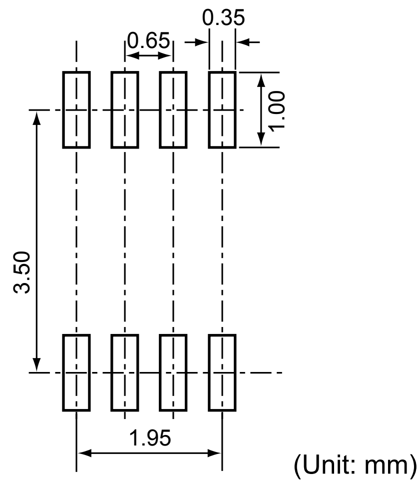
(Unit: mm)

● **SC-82AB**



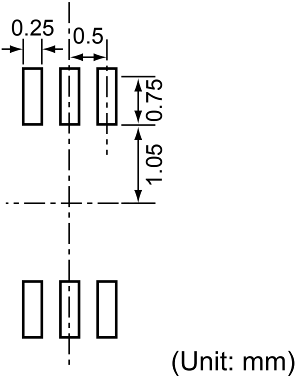
(Unit: mm)

● **SSOP-8G**



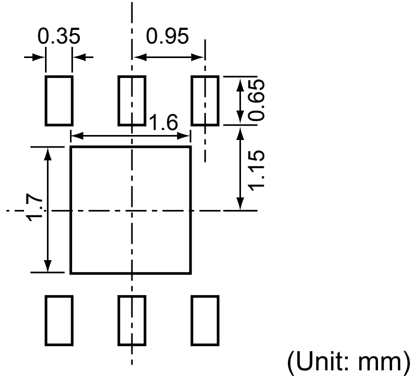
(Unit: mm)

- **SON-6**



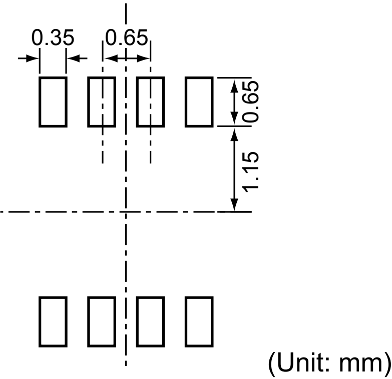
(Unit: mm)

- **HSON-6**



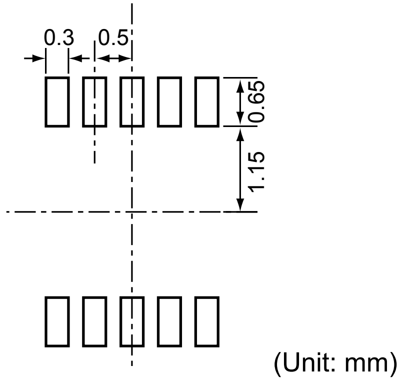
(Unit: mm)

- **SON-8**



(Unit: mm)

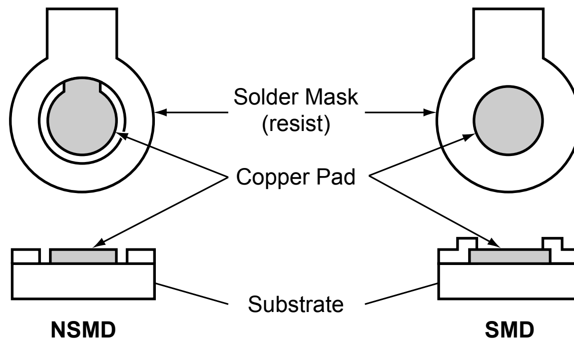
- **SON-10**



(Unit: mm)

*Pad layout and size can be modified by customers material, equipment, method.
*Please adjust pad layout according to your conditions.

- **WL-CSP**

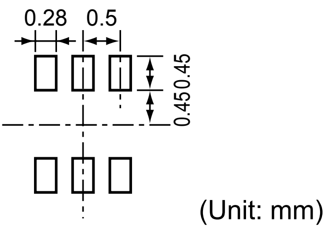


NSMD and SMD Pad Definition

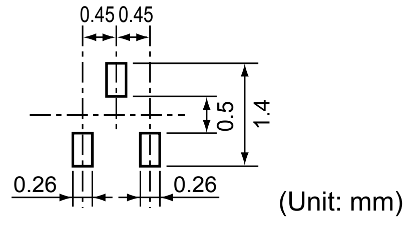
Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.20mm	Min. 0.30mm
SMD (Solder Mask defined)	Min. 0.30mm	0.20mm

* Pad layout and size can be modified by customers material, equipment, method.
* Please adjust pad layout according to your conditions.
* Recommended Stencil Aperture Size....ø0.3mm
* Since lead free WL-CSP components are not compatible with the tin/lead solder process, you shall not mount lead free WL-CSP components using the tin/lead solder paste.

● **SON1612-6**



● **SON1408-3**



● **PLP1820-6**